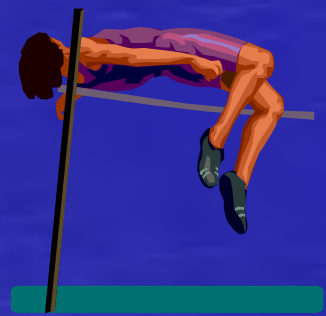
Overcoming the Red Brick Walls

Paolo Gargini
Chairman ITRS
IEEE Fellow
Director of Technology Strategy
Intel Fellow

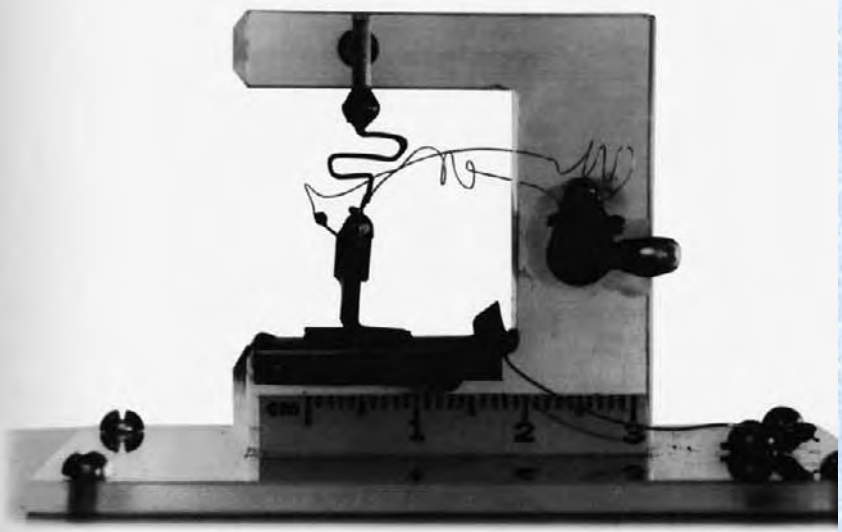


2008 ISS US

Agenda

- Yesterday
- Today
- Tomorrow
- The Day after Tomorrow

The First Bipolar Transistors



1947. J. Bardeen and W. Brattain

"…failures of attempts to make field-effect transistors became <creative failures> by creating the program that discovered the point-contact transistor"

1963. W. B. Shockley

"…Bardeen and I were simply trying to make a good <Field Effect> device and as a result we were put in the position to observe, for the first time, a phenomenon now called the <Transistor Effect> and to use this to make a transistor".

1974. W. Brattain

1948. W.B. Shockley

The first junction transistor.

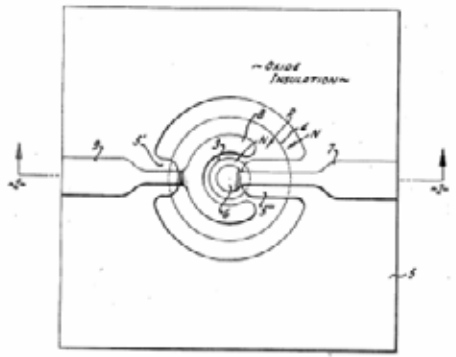
The First Planar Integrated Circuit 1961

April 25, 1961 R. N. NOYCE 2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959 3 Sheets-Sheet 1

FIG-1



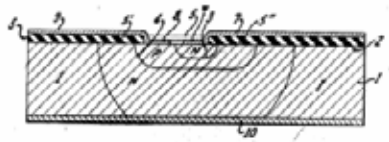
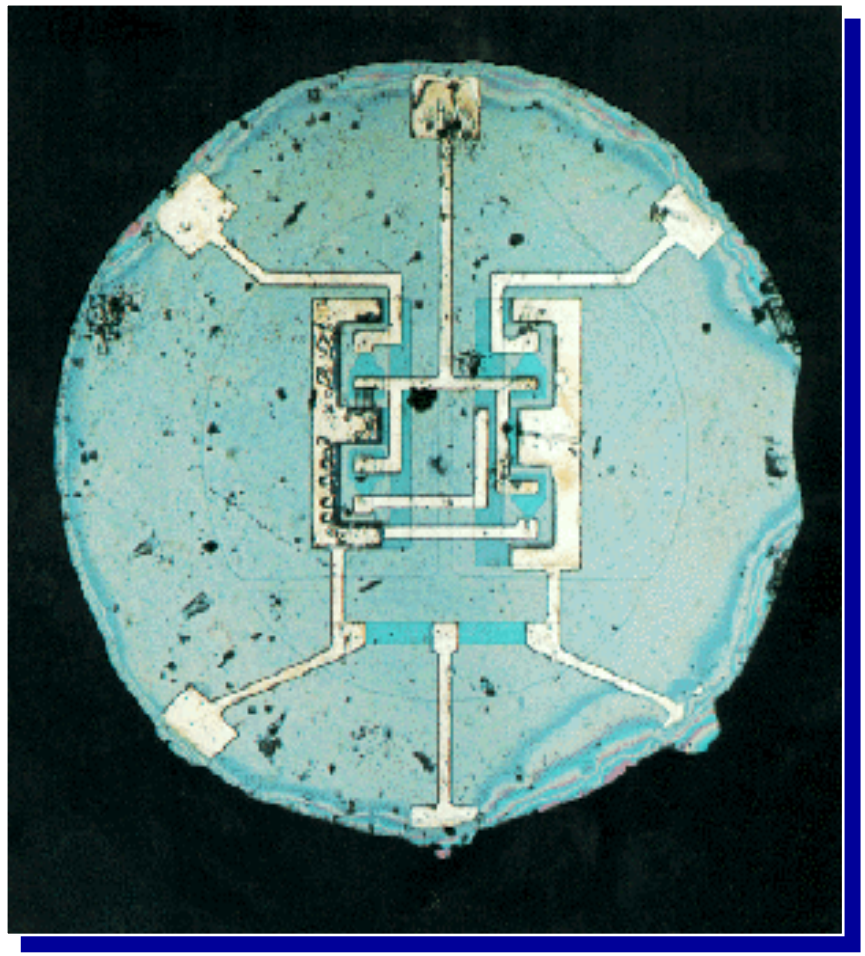
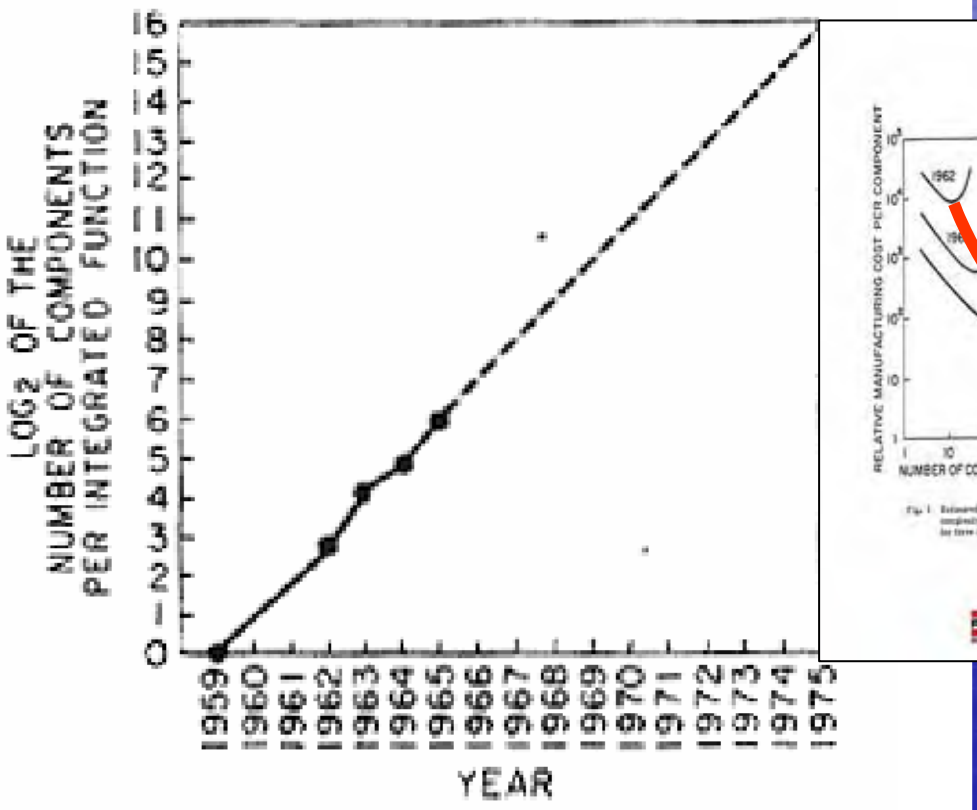


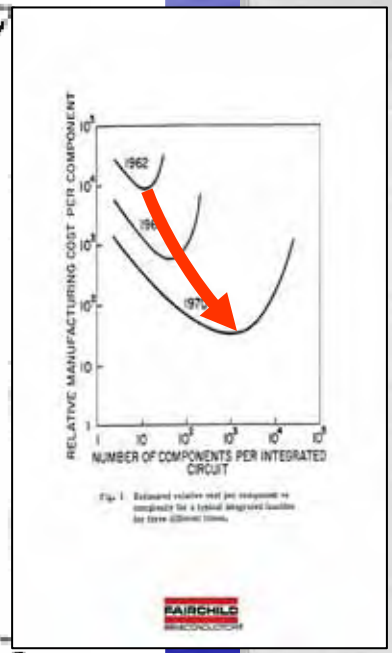
FIG-2

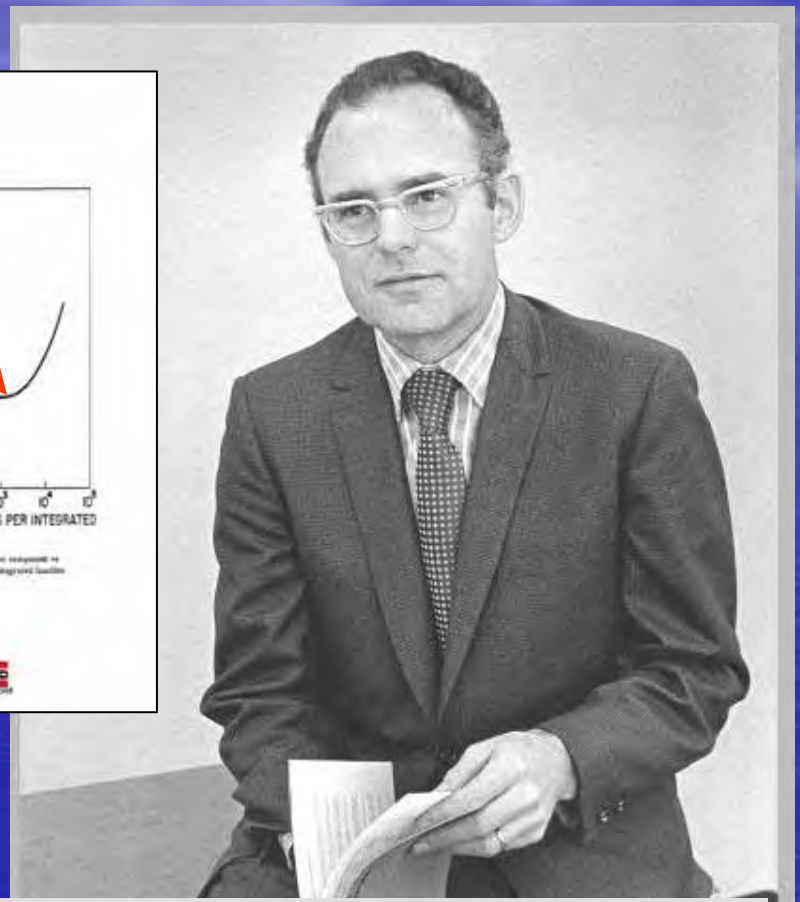
INVENTOR.
ROBERT N. NOYCE
BY Lappin & Kalb
ATTORNEYS



Moore's Law - 1965







"**<u>Reduced cost</u> is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."**
Electronics, Volume 38, Number 8, **April 19, 1965**

1967: Minimizing Surface States

J. Electrochem. Soc.: SOLID STATE SCIENCE *March 1967*

Characteristics of the Surface-State Charge (Q_{ss}) of Thermally Oxidized Silicon

B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow

Research and Development Laboratories, Fairchild Semiconductor, Palo Alto, California

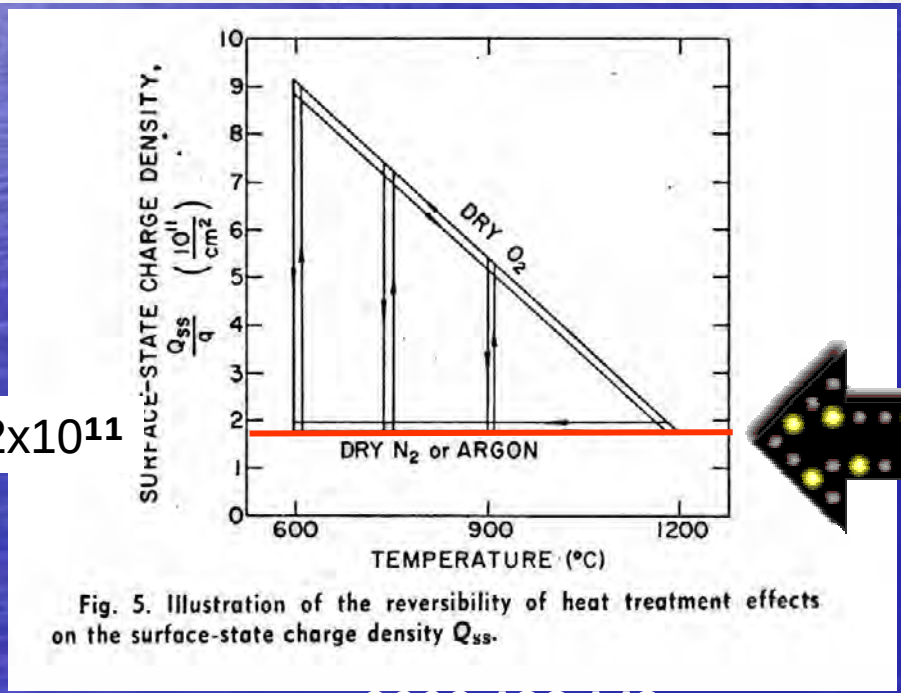
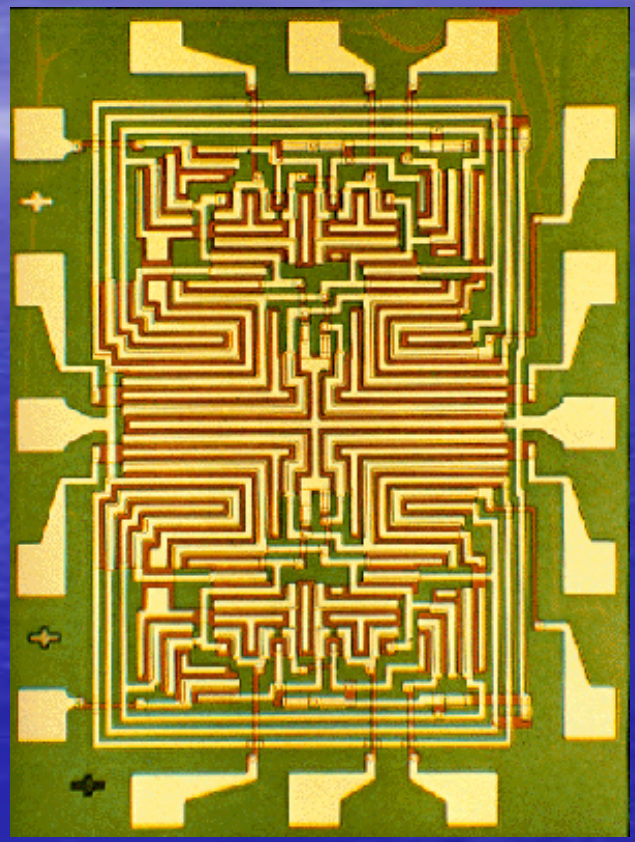


Fig. 5. Illustration of the reversibility of heat treatment effects on the surface-state charge density Q_{ss}.

$2x10^{11}$

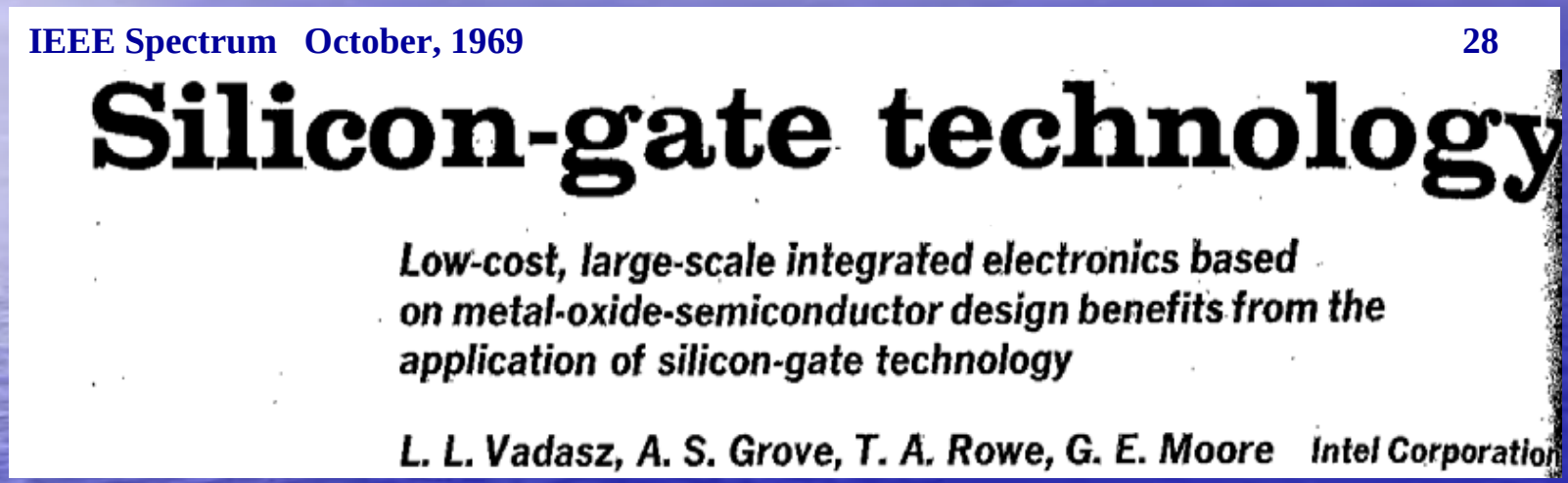
The MOS Integrated Circuit Takes Off in 1966

- Fairchild's first MOS integrated circuit product – a dual J-K flip-flop.



FAIRCHILD
SEMICONDUCTOR®

The Silicon Gate Takes Off!



IEEE Spectrum October, 1969 28

Silicon-gate technology

Low-cost, large-scale integrated electronics based on metal-oxide-semiconductor design benefits from the application of silicon-gate technology

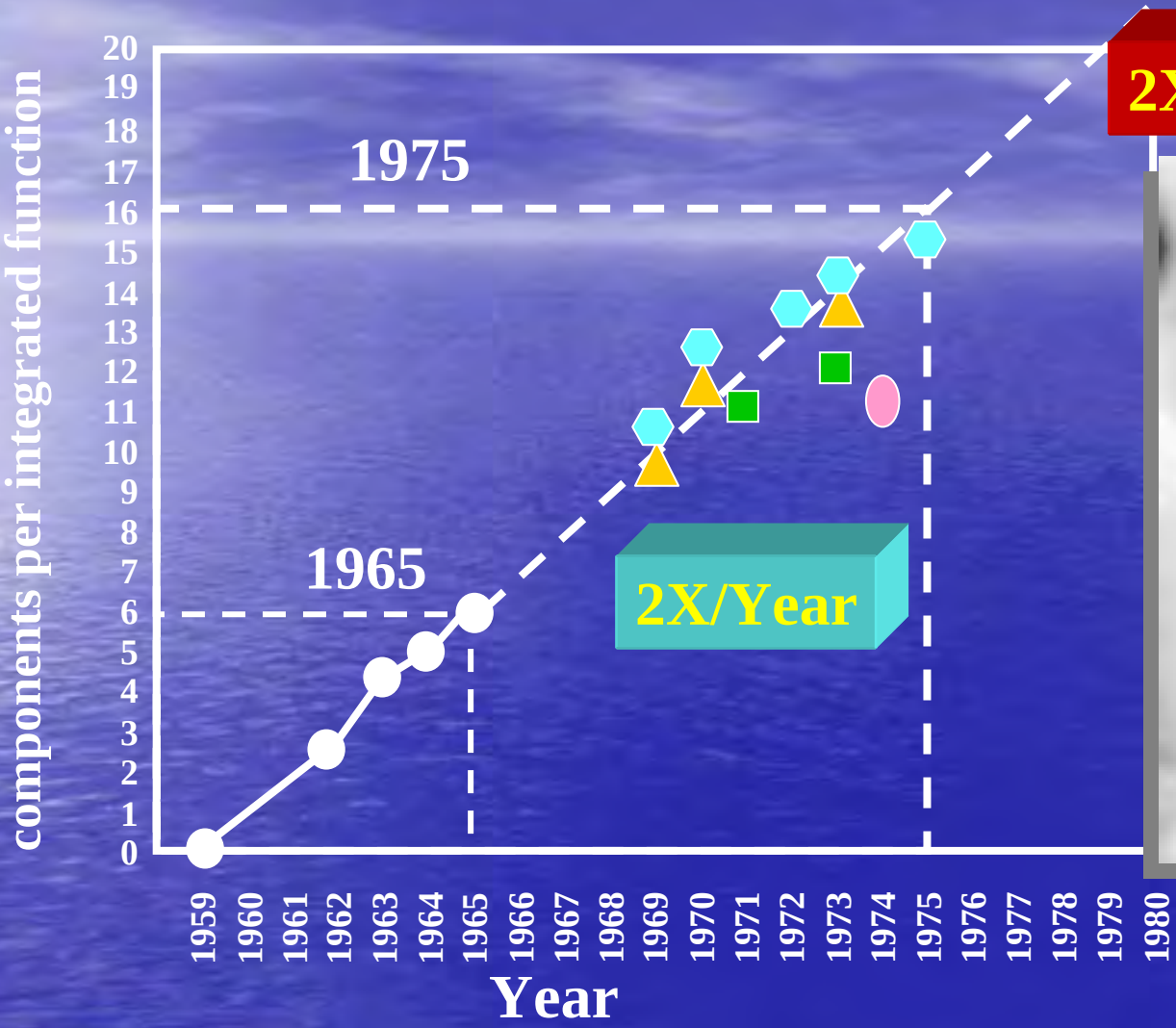
L. L. Vadasz, A. S. Grove, T. A. Rowe, G. E. Moore Intel Corporation

intel

Commercialization of MOS

- 1969. 1101, 6T, 256 SRAM produced
- 1970. 1103, 3T, 1Kbit DRAM produced
- 1971. 2101/2, 6T, 1Kbit SRAM produced
- 1971. 1702, 2Kbit EPROM produced
- 1971. 4004 MPU produced
- 1972. 2104,1T, 4Kbit DRAM produced

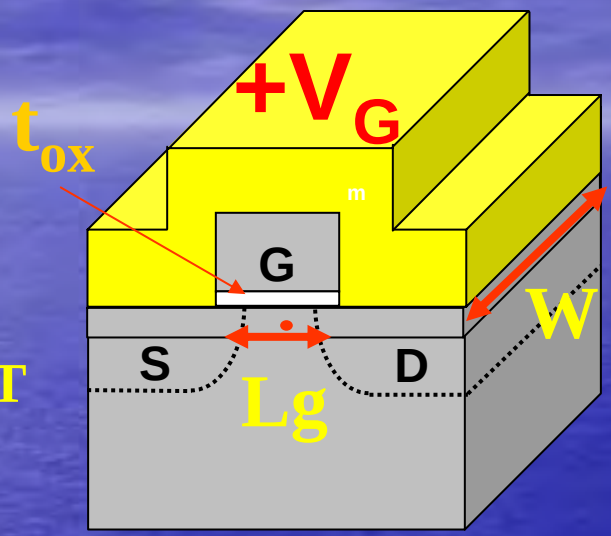
Second Update of Moore's Law



International Electron Device Meeting, December 1975

2008 ISS US

Transistor Components



$V_G = V_D = V_{DD} - V_T$

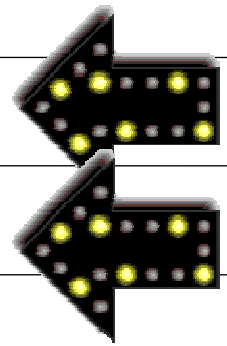
Vertical | Horizontal | Performance

$$\frac{I_{DSat}}{W} \sim \frac{1}{2}\left[\frac{\varepsilon_o\,\varepsilon_s}{t_{ox}}\right]\left[\frac{\mu}{Lg}\right](V_{DD} - V_T)^2$$

Charge | Density | Power

1994 NTRS

	1995 0.35 µm	*1998 0.25 µm*	*2001 0.18 µm*	*2004 0.13 µm*	*2007 0.10 µm*	*2010 0.07 µm*
Isolation	**LOCOS/ STI †/SOI**	**STI †/SOI**				
Gate oxide	**thermal**	**thermal/rapid thermal oxidation**				
Gate electrode		**n; n/p poly; poly/ silicide**				
Source/drain	**LDD*/MDD ‡; S/D ext**	**same + raised S/D**				
Interconnect	**planar**					
Wires	**Al based**	**Al, Cu (thick)**				
Interlevel dielectric	**oxide**	**oxide; air; polyimide; low dielectric**				
Via studs	**W**	**W/Al/Cu**				

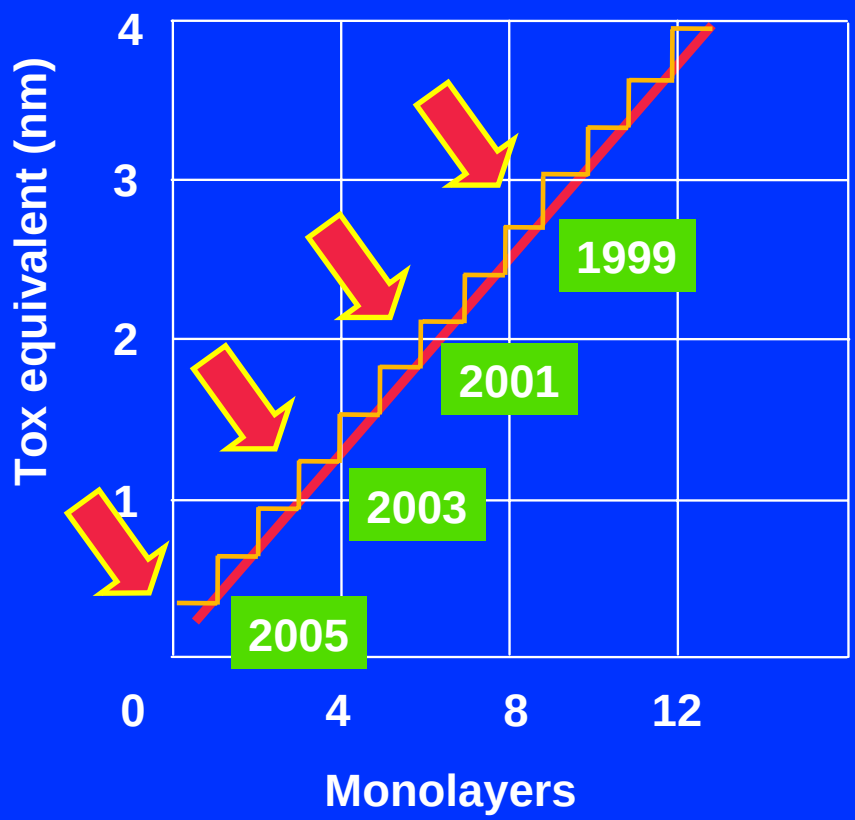


**LDD - lightly doped drain*
†STI - shallow trench isolation
‡MDD - medium doped drain

Table 6 Logic Technology Characteristics

From My Files

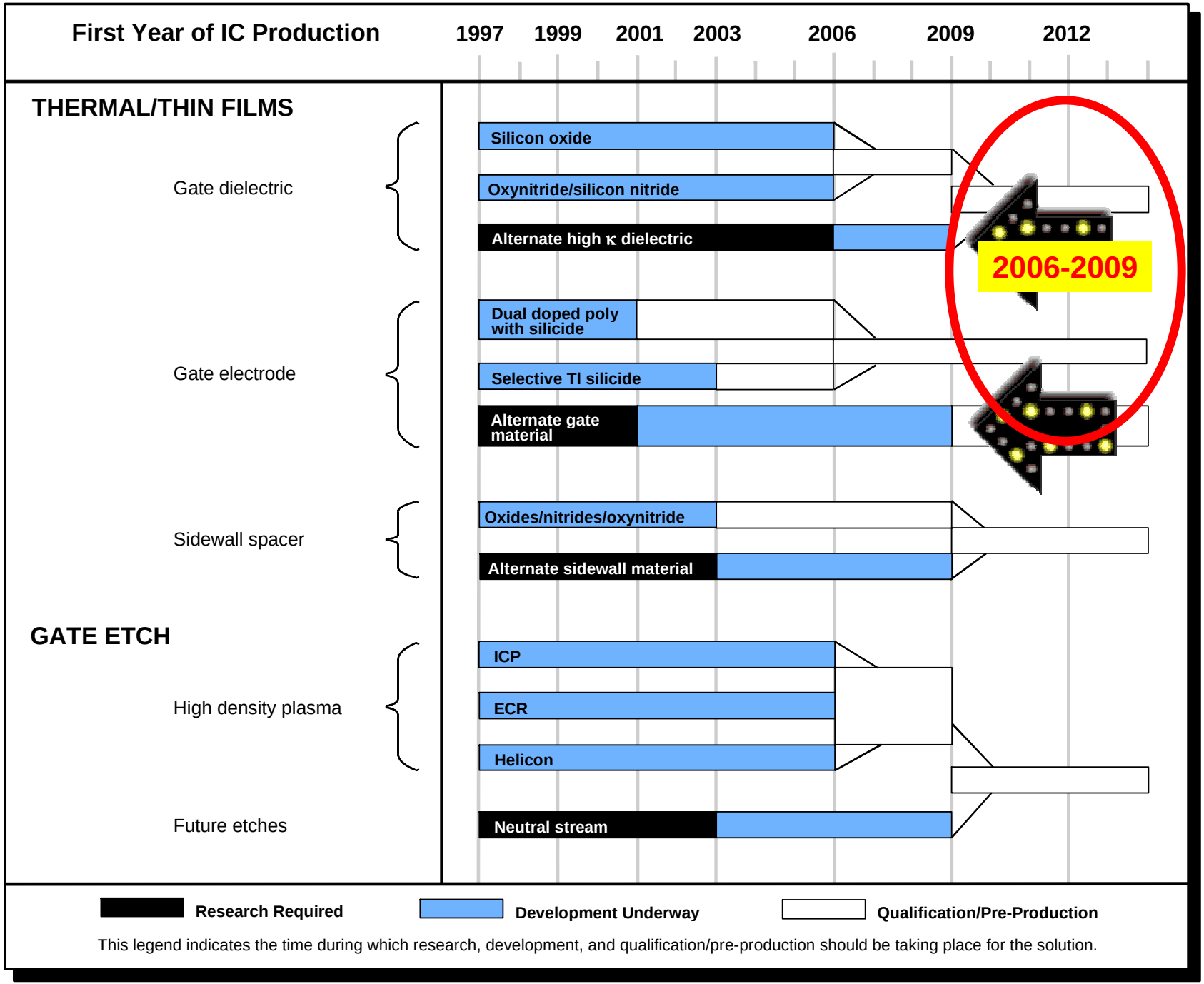
Gate Dielectric Scaling



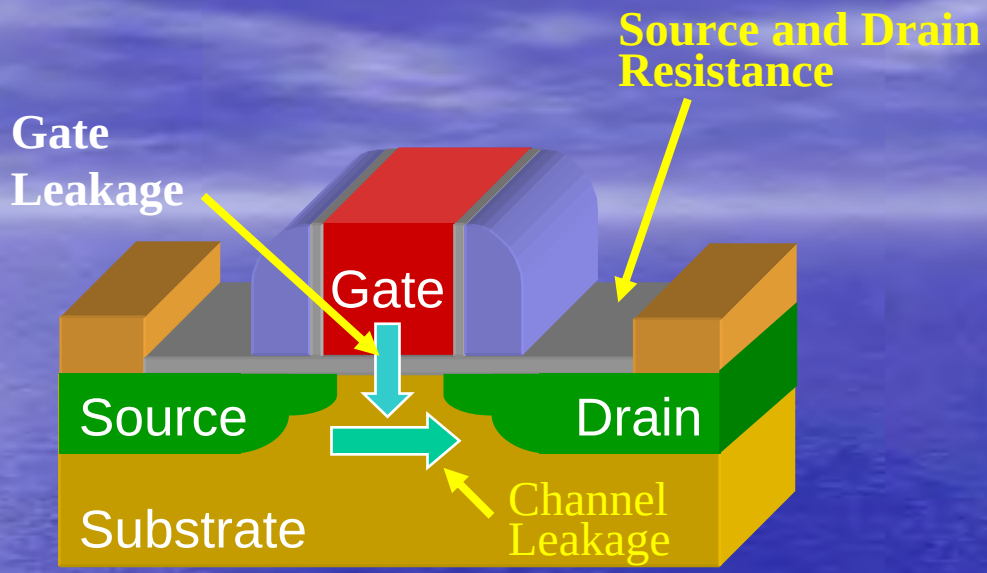
1997 NTRS

P.Gargini

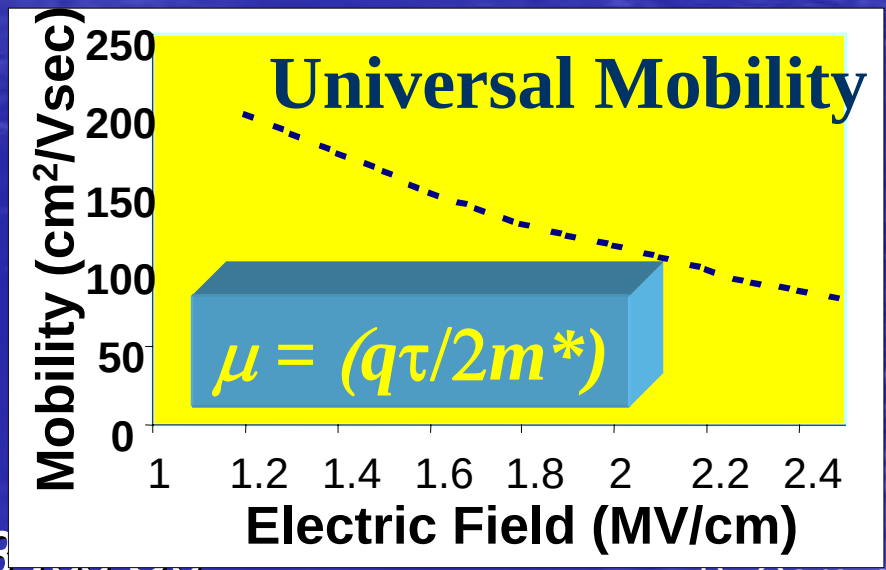
1997 NTRS


First Year of IC Production
1997
1999
2001
2003
2006
2009
2012
THERMAL/THIN FILMS
Gate dielectric
Silicon oxide
Oxynitride/silicon nitride
Alternate high κ dielectric
2006-2009
Gate electrode
Dual doped poly with silicide
Selective Tl silicide
Alternate gate material
Sidewall spacer
Oxides/nitrides/oxynitride
Alternate sidewall material
GATE ETCH
High density plasma
ICP
ECR
Helicon
Future etches
Neutral stream
Research Required
Development Underway
Qualification/Pre-Production
This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

Geometrical Scaling Limitations



- S/D Leakage
- Gate Leakage
- S/D Resistance
- Decreased Mobility



1998 ITRS Update

- Participation extended to: EECA, EIAJ, KSIA, TSIA at WSC on April 23,1998
- 1st Meeting held on July 10/11,1998 in San Francisco
- 2nd meeting held on December 10/11,1998 at SFO
- 50% of tables in 1997 NTRS required some changes
- 1998 ITRS Update posted on web in April 1999

P.Gargini

CMOS Future Directions

1970-2004

Traditional Scaling → 70%/2-3year

Features

2005-2014

Equivalent Scaling → 70% / 2-3year → Innovation

2000-2014

Integrated Solutions → 2X Perf → SOC, SIP, 3D

2010-20XX

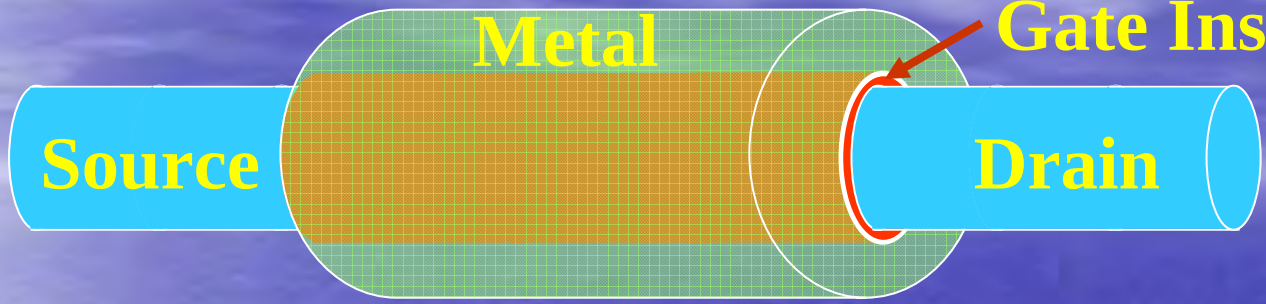
New Devices → Nanotech

From My Files

ITRS 7/11/1998

ITRS US

The Ideal MOS Transistor



Fully Surrounding Metal Electrode

Fully Enclosed, Depleted Semiconductor

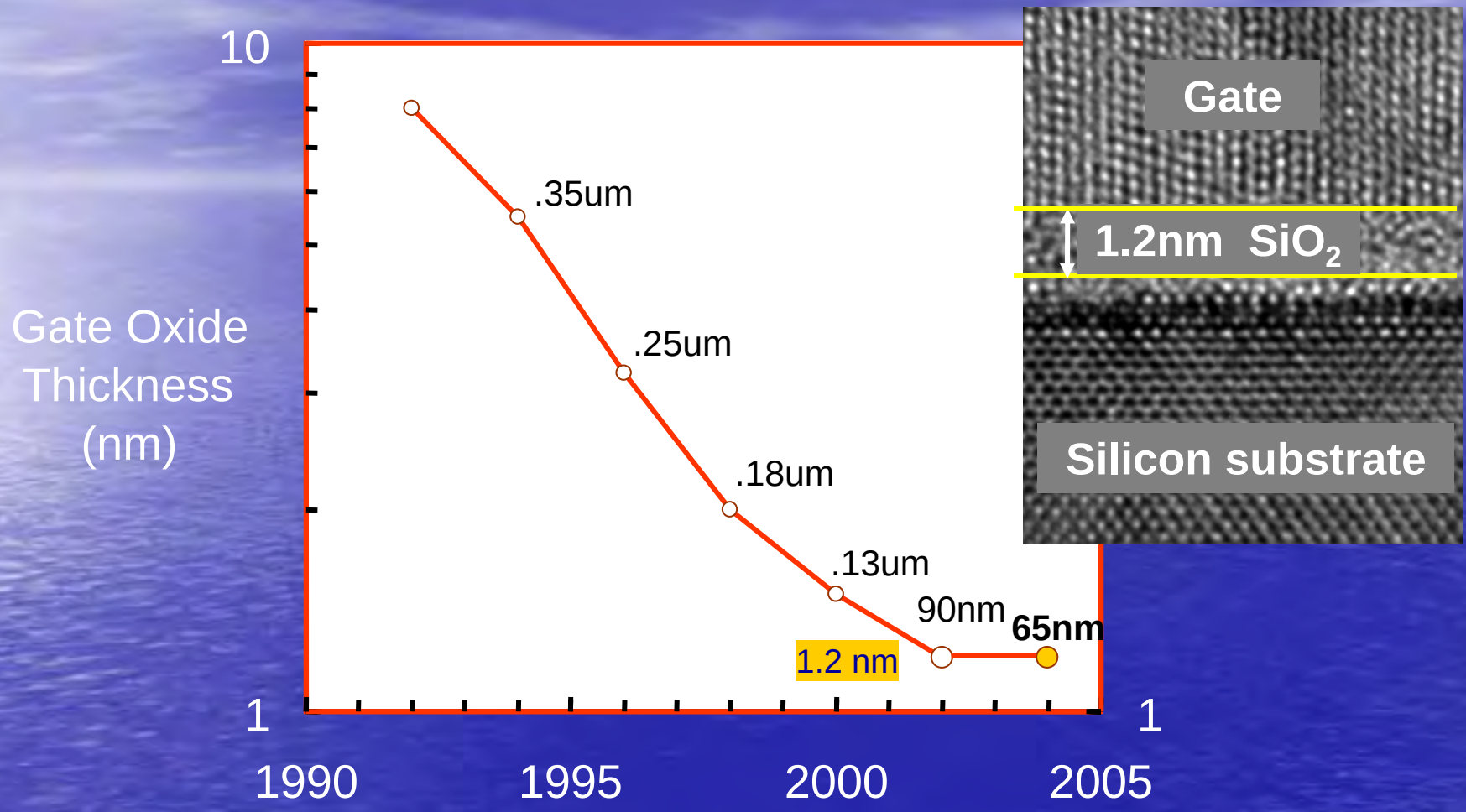
High-K Gate Insulator

Low Resistance Source/Drain

Band Engineered Semiconductor

From My Files

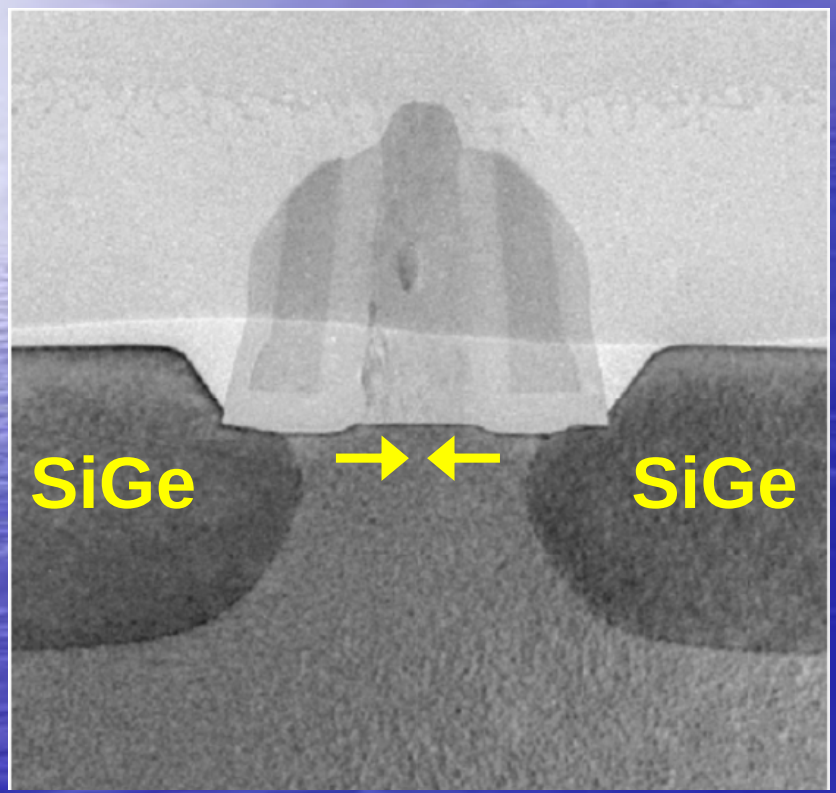
Gate Oxide Scaling



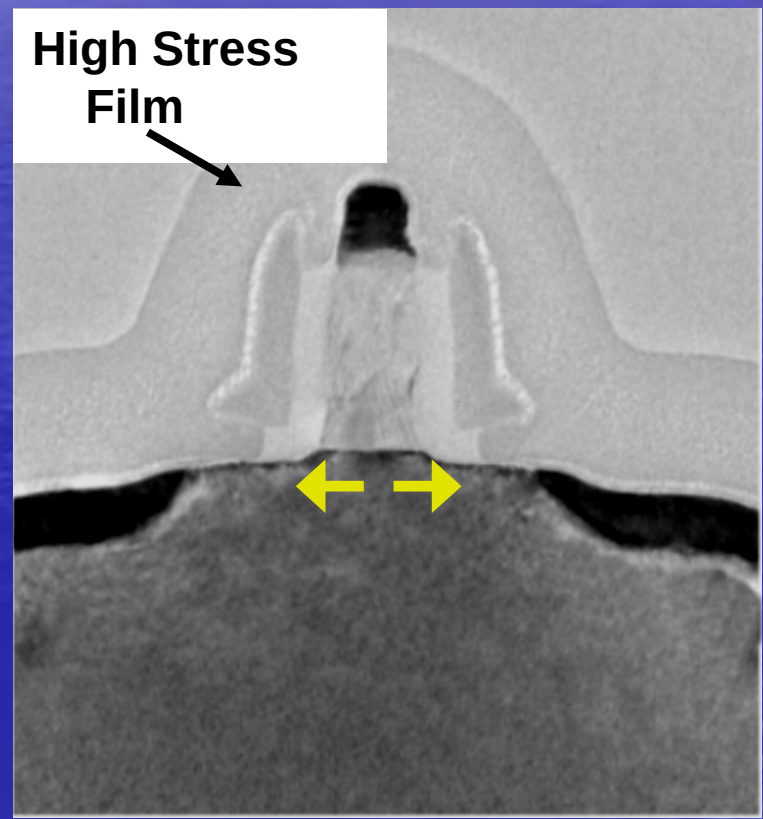
Gate oxide scaling is reaching its limits

Mobility Innovation

Strained P-Channel Transistor



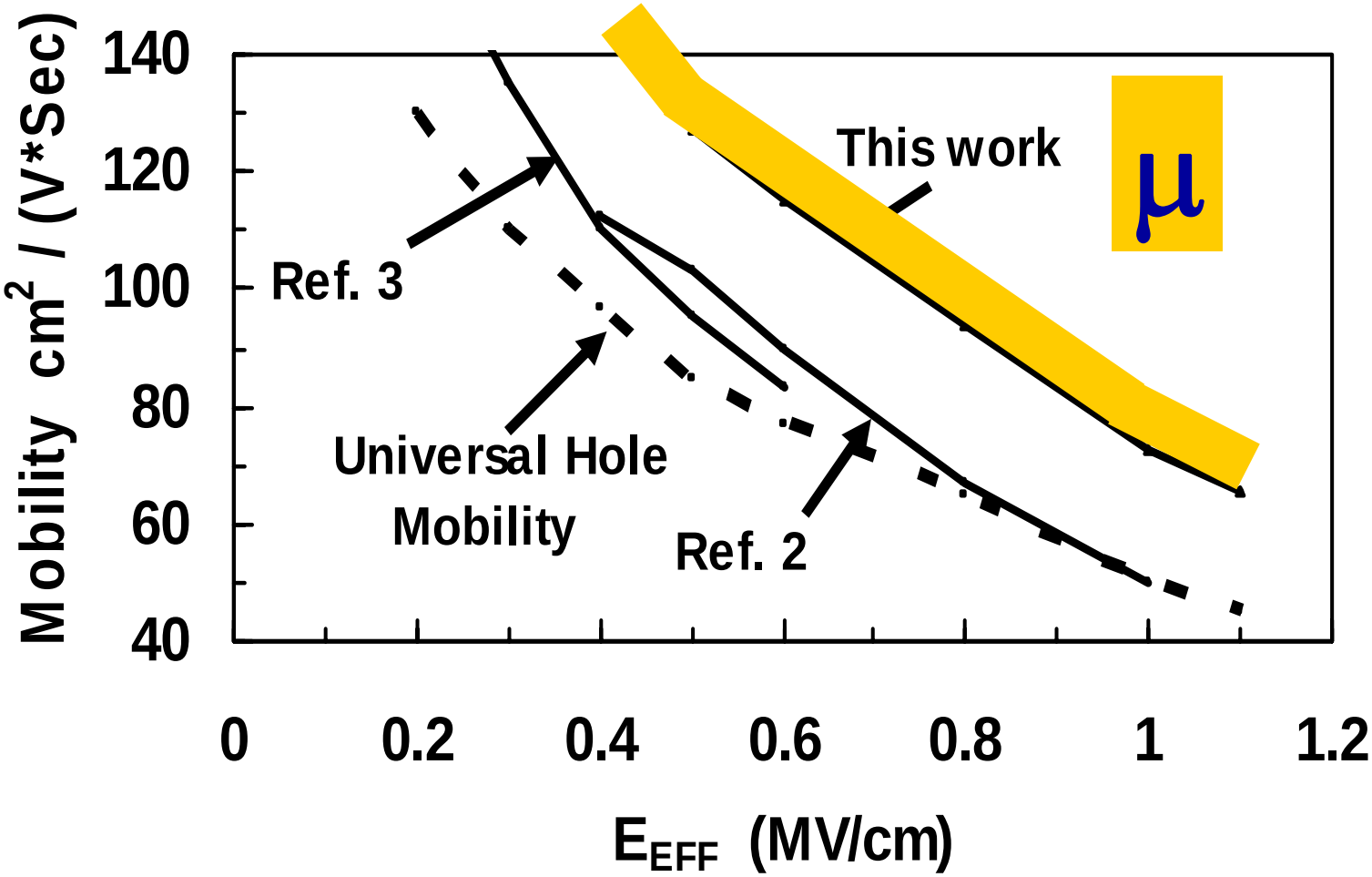
Strained N-Channel Transistor



2008 ISS US

Source: Intel

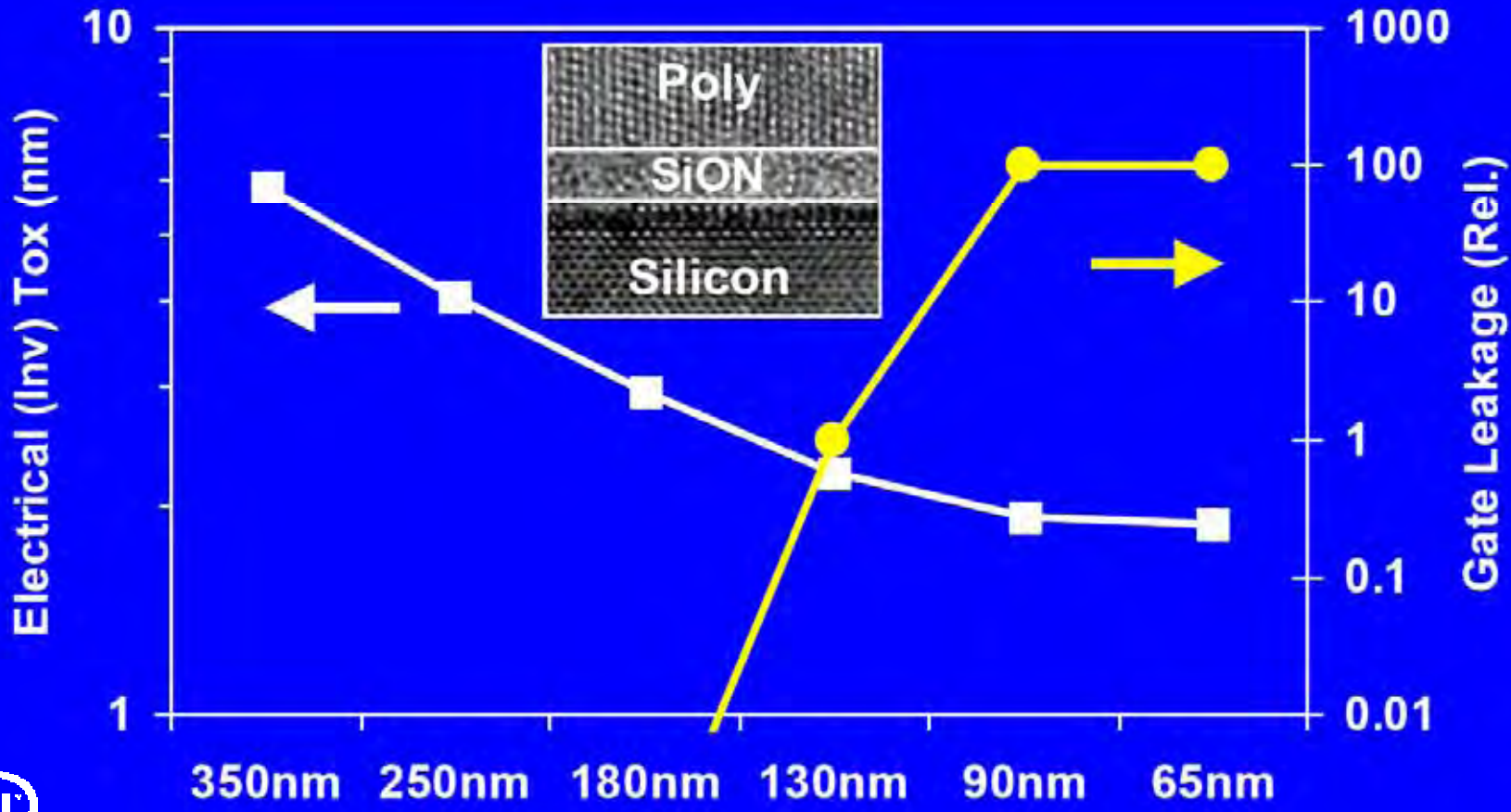
Hole Mobility as a Function of Vertical Effective Field



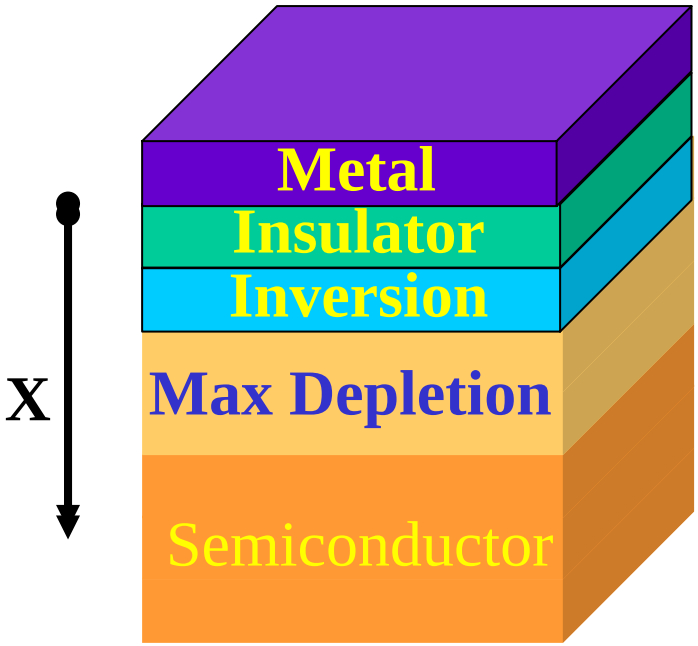
Source: T. Ghani, 2003 IEDM

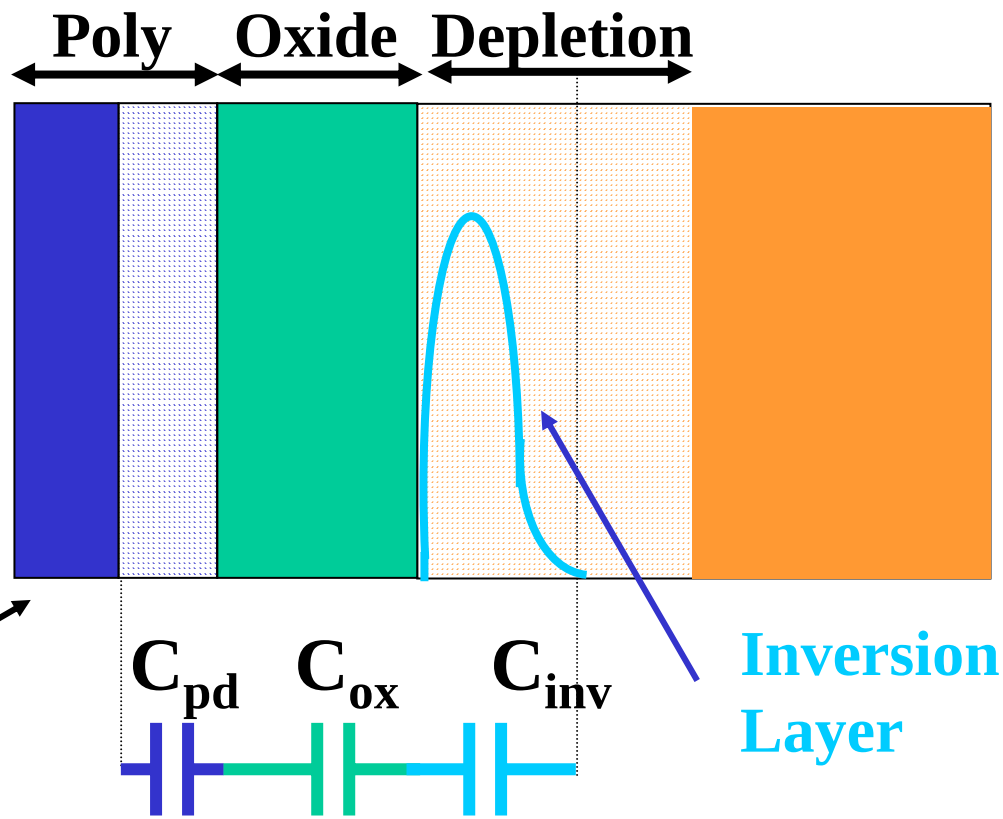
Problem Statement

- SiON scaling running out of atoms
- Poly depletion limits inversion T_{OX} scaling



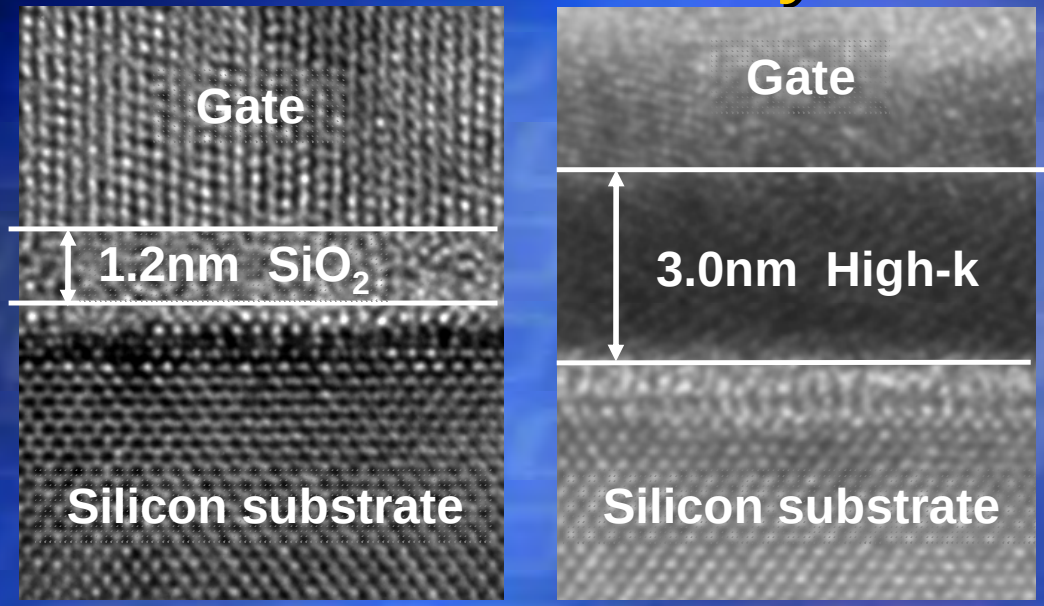
Capacitance Reduction





=>Metal Gate is needed to eliminate polysilicon depletion

High-k Dielectric reduces leakage substantially



Benefits compared to current process technologies

	High-k vs. SiO_2	Benefit
Capacitance	60% greater	*Much faster transistors*
Gate dielectric leakage	> 100x reduction	*Far cooler*

Continuation of Moore's Law

Process Name	P856	P858	Px60	P1262	P1264	P1266	P1268	P1270
1st Production	1997	1999	2001	2003	2005	2007	2009	2011
Process Generation	0.25μm	0.18μm	0.13μm	90 nm	65 nm	45 nm	32 nm	22 nm
Wafer Size (mm)	200	200	200/300	300	300	300	300	300
Inter-connect	Al	Al	Cu	Cu	Cu	Cu	Cu	?
Channel	Si	Si	Si	Strained Si	Strained Si	Strained Si	Strained Si	Strained Si
Gate dielectric	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	High-k	High-k	High-k
Gate electrode	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Metal	Metal	Metal

Introduction targeted at this time

Subject to change

R.Chau

Intel found a solution for High-k and metal gate

Agenda

- Yesterday
- Today
- Tomorrow
- The Day after Tomorrow

A 45nm Logic Technology with High-k + Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging

K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau*, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He#, J. Hicks#, R. Heussner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz#, B. McIntyre, P. Moon, J. Neirynck, S. Pae#, C. Parker, D. Parsons, C. Prasad#, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren%, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, K. Zawadzki

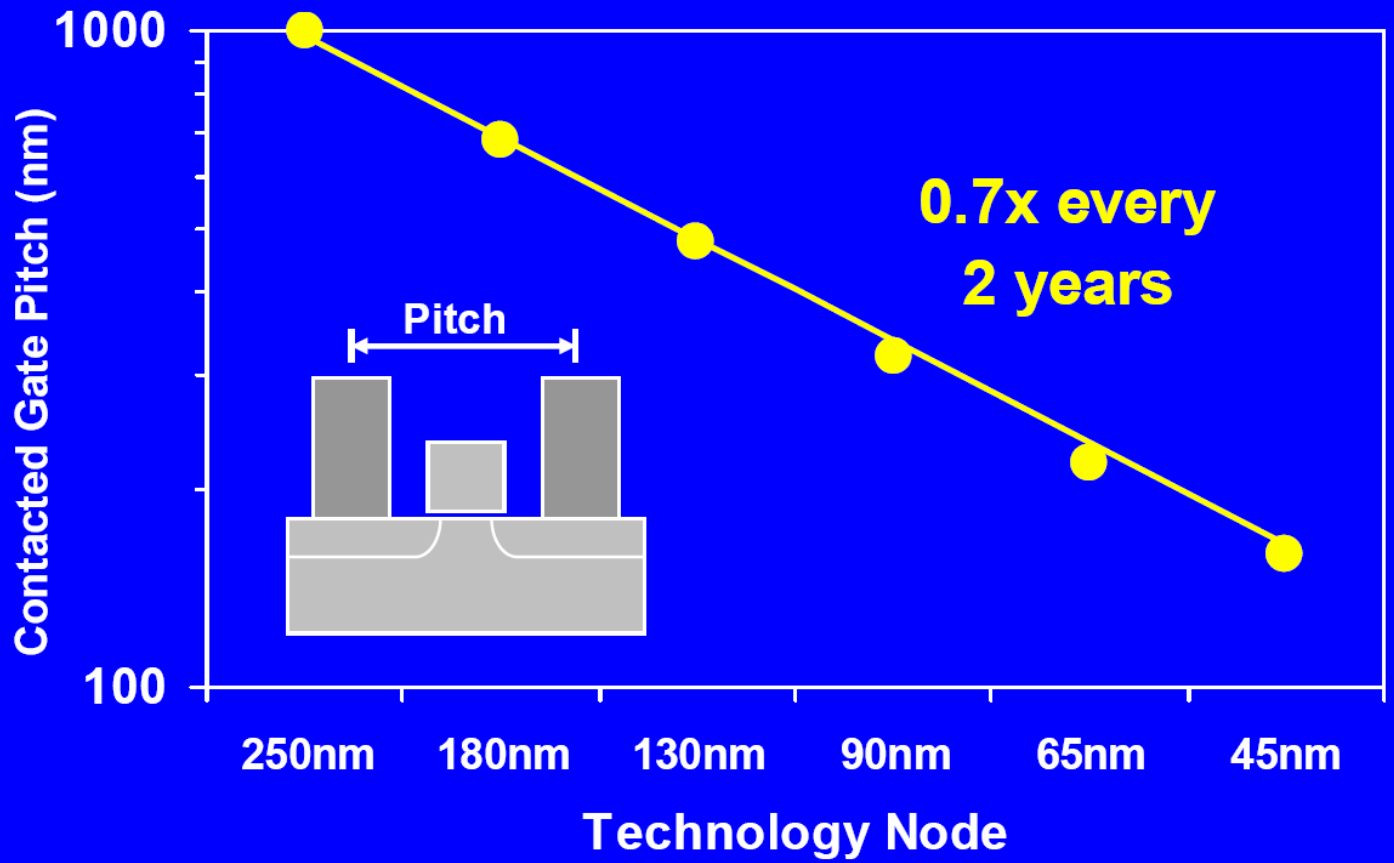
Portland Technology Development, *CR, #QRE, %PTM

Intel Corporation

IEDM 2007

Contacted Gate Pitch

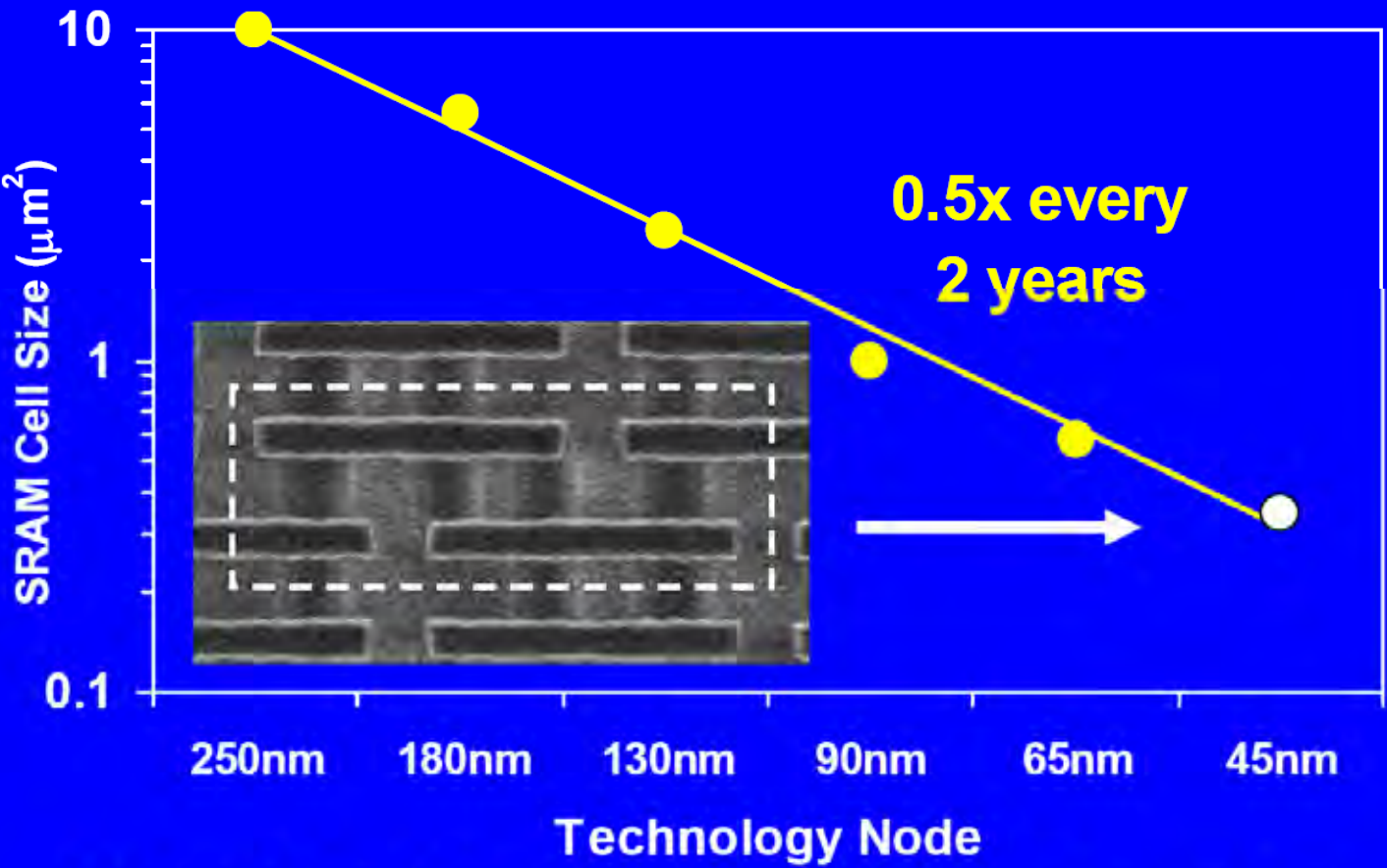
- Transistor gate pitch of 160 nm continues 0.7x per generation scaling



Tightest contacted gate pitch reported for 45 nm generation

SRAM Cells

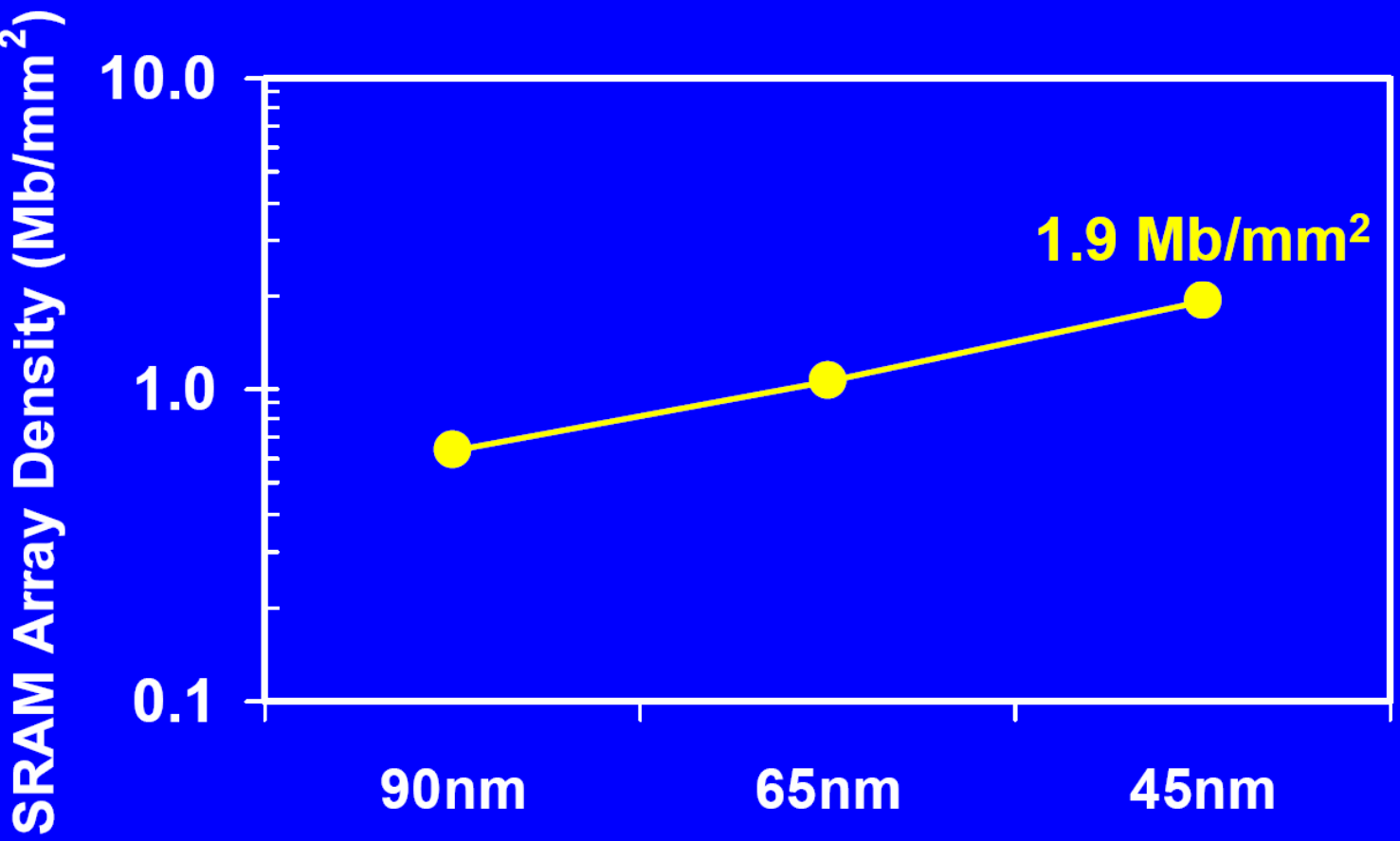
- 0.346 μm² and 0.382 μm² SRAM cells
  - Optimize density and power/performance



Transistor density doubles every two years

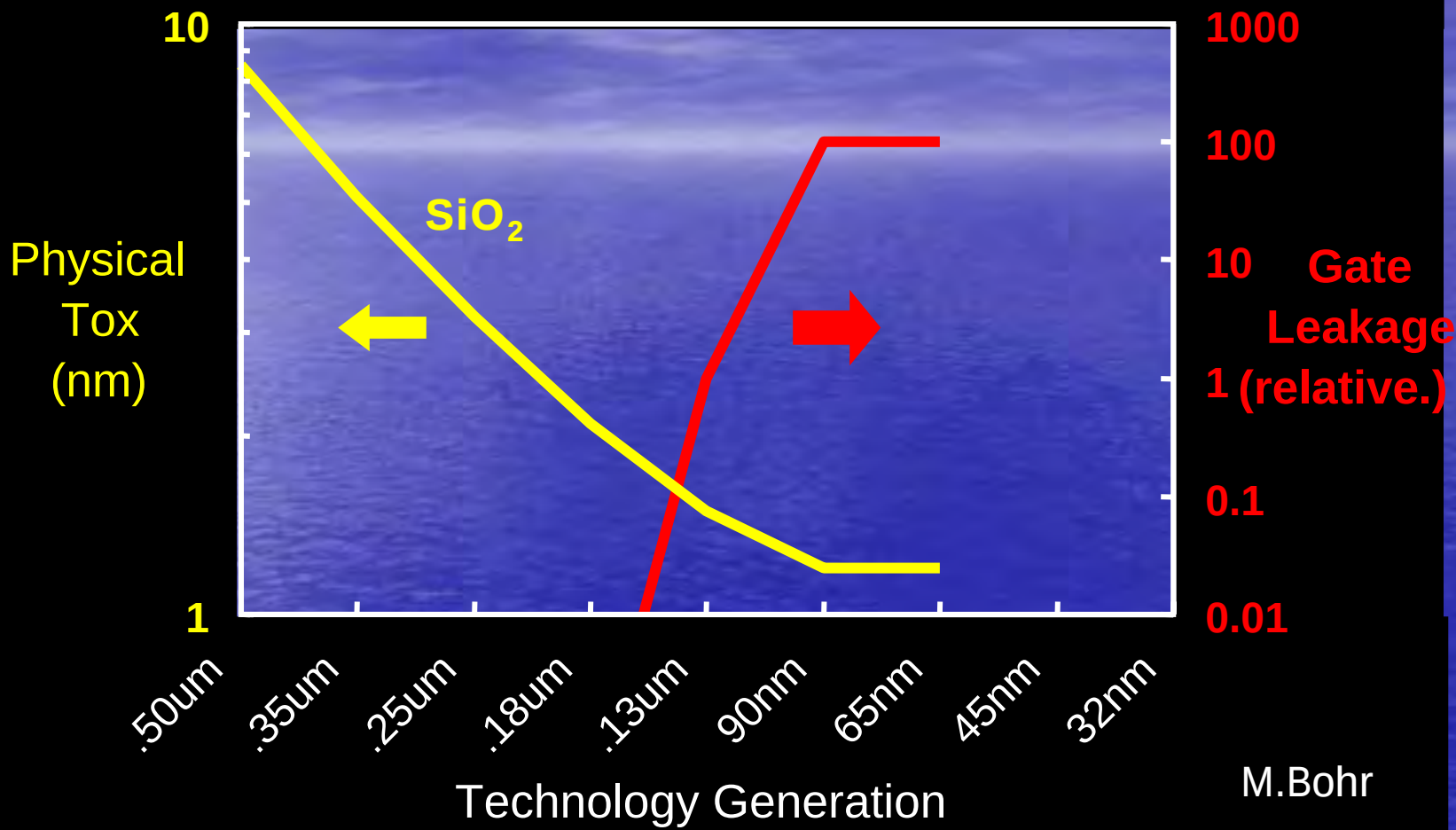
SRAM Array Density

- SRAM array density achieves 1.9 Mb/mm^2
  - Includes row/column drivers and other circuitry



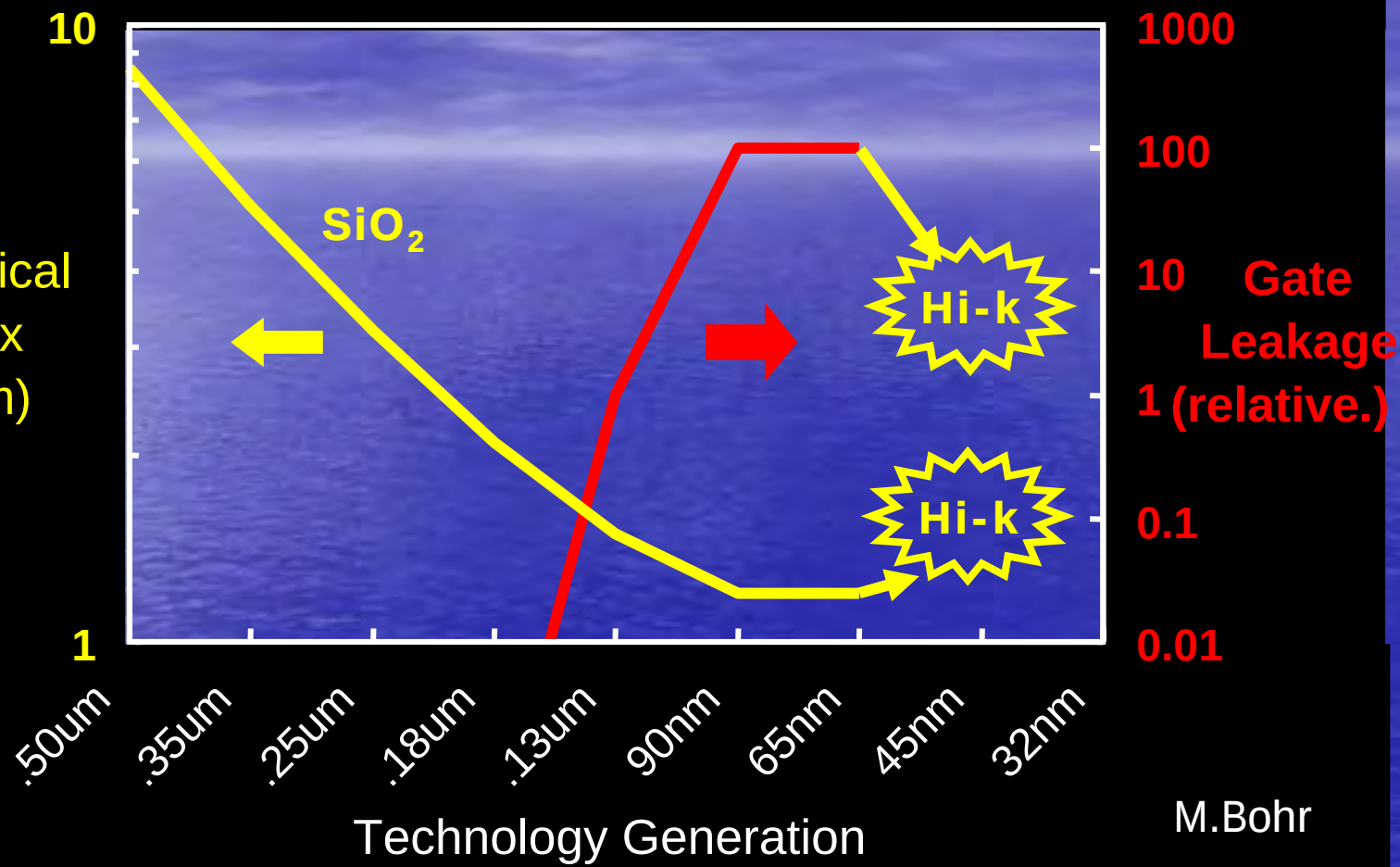
Array density scales at ~2X per generation

Gate Oxide Leakage



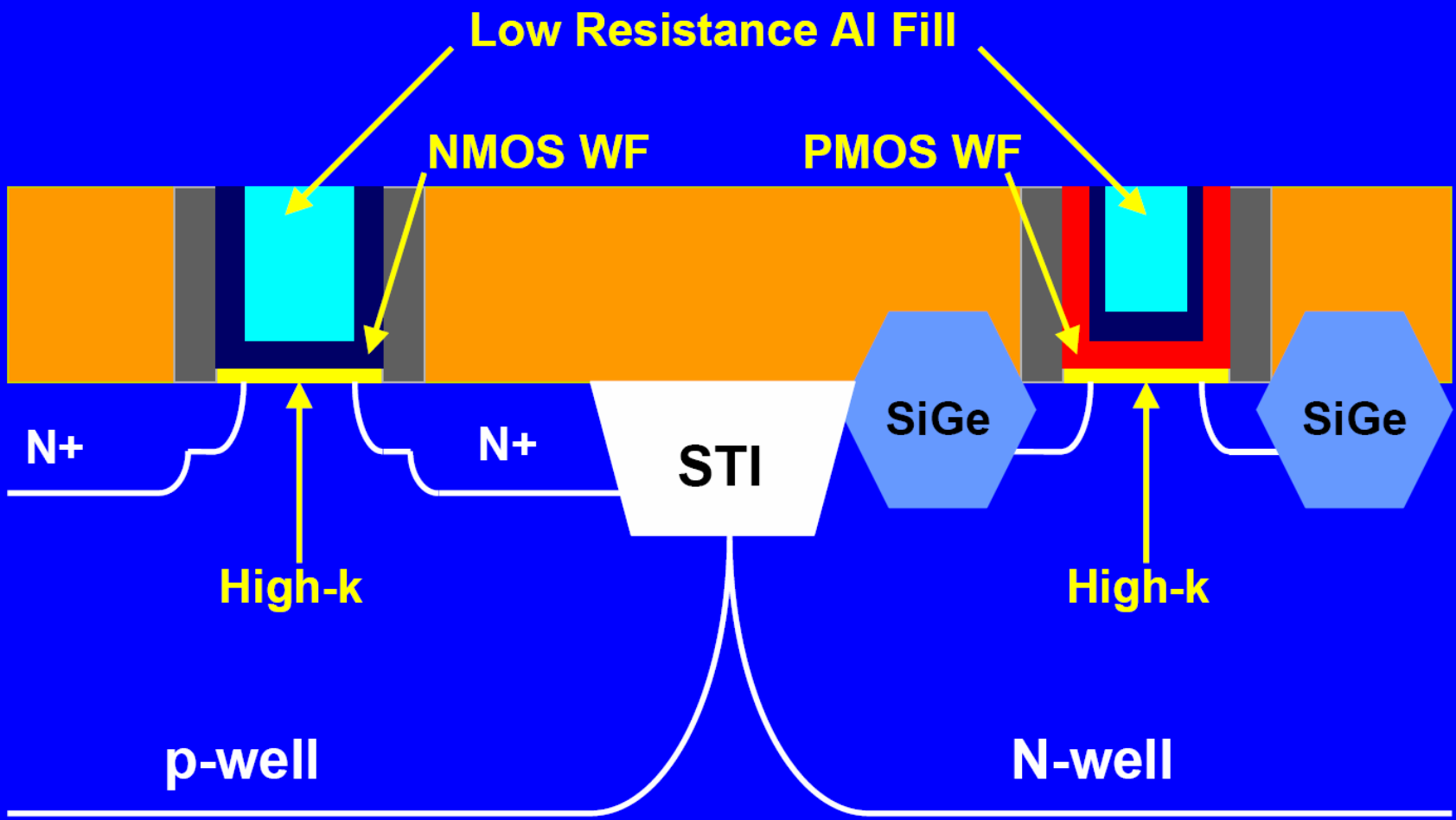
Gate oxide scaling stopped due to leakage

Gate Oxide Leakage



High-k dielectric breaks through this barrier

Transistor Process Flow



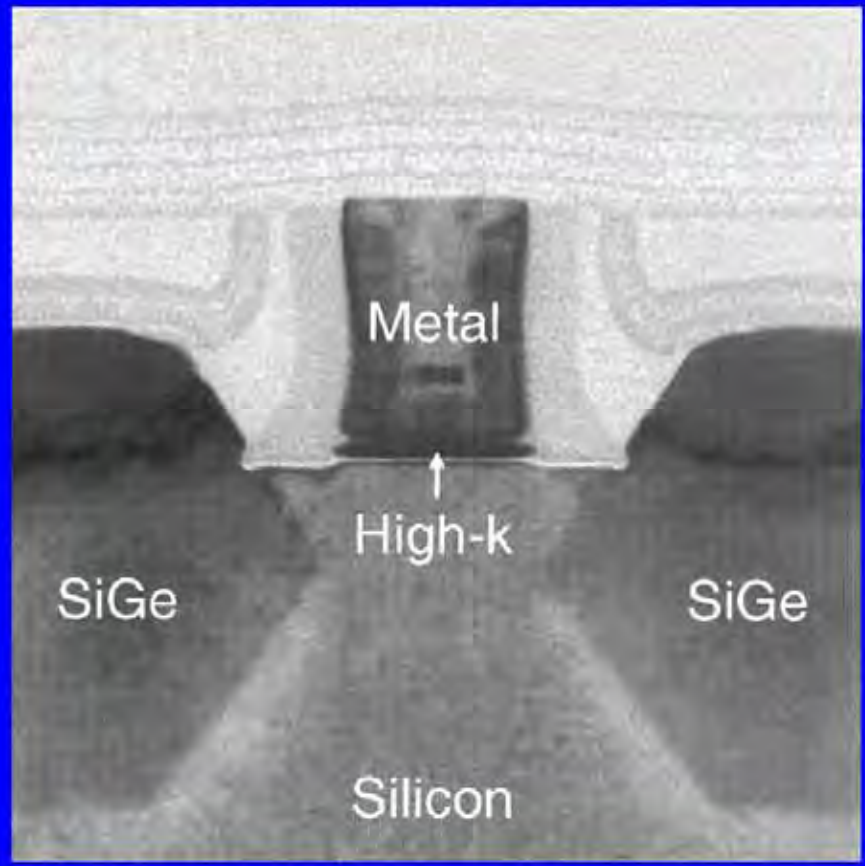
High-k + Metal gate transistor formation complete

Transistor Features

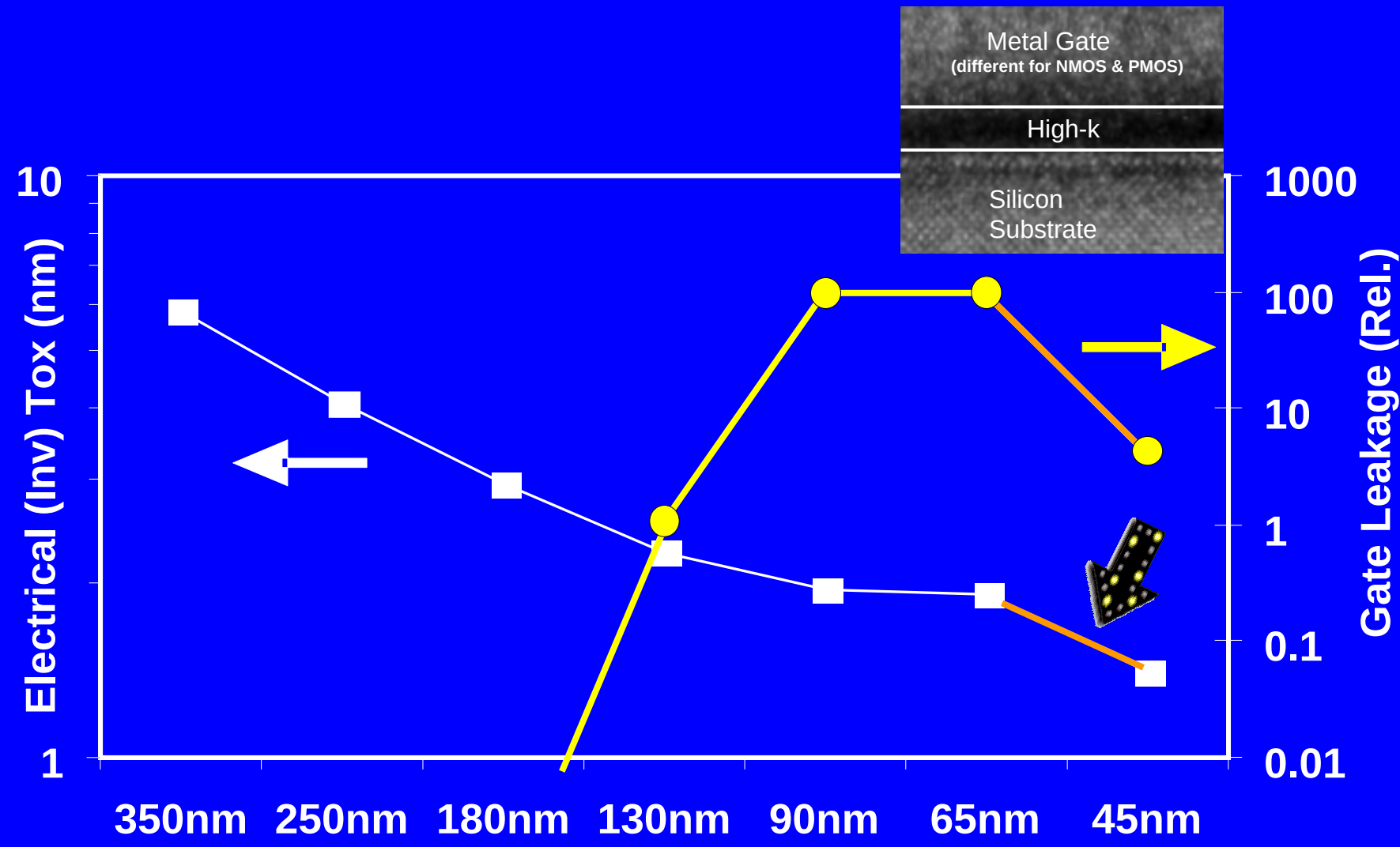
- 35 nm min. gate length
- 160 nm contacted gate pitch

- 1.0 nm EOT Hi-K
- Dual workfunction metal gate electrodes

- 3RD generation of strained silicon

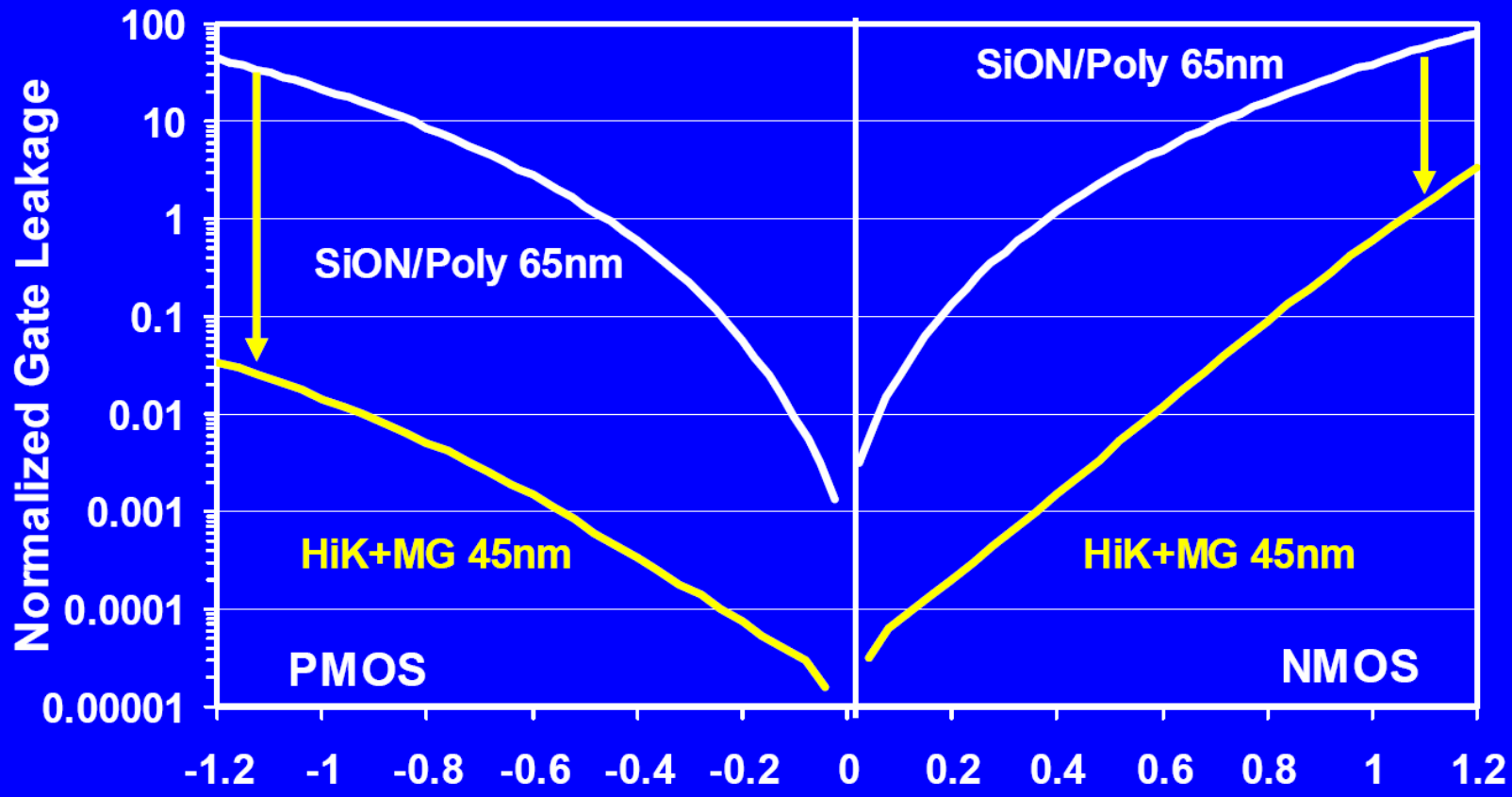


Scaling trend for inversion electrical TOX



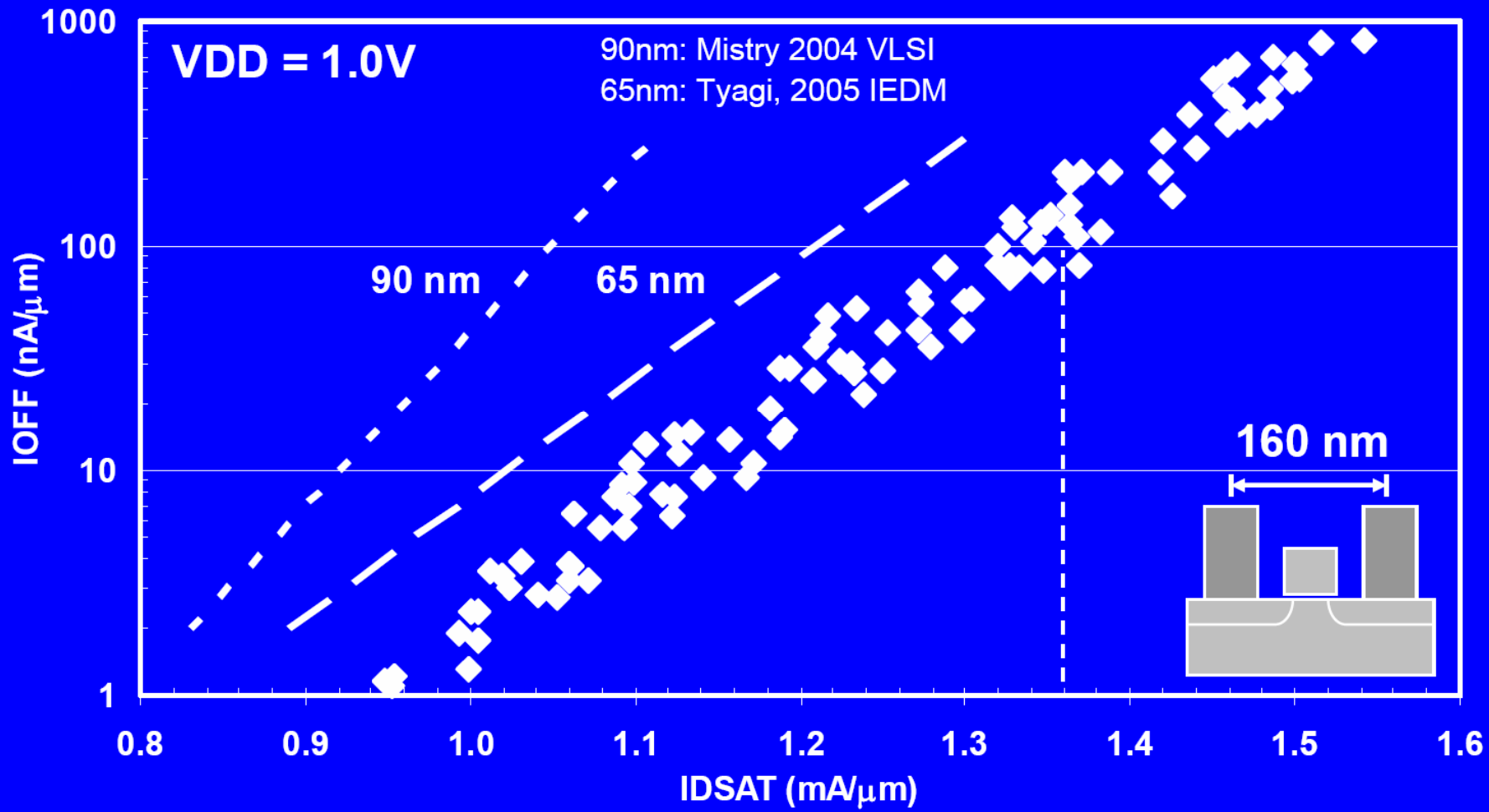
Gate Leakage

- Gate leakage is reduced >25X for NMOS and 1000X for PMOS



65nm: Bai, 2004 IEDM

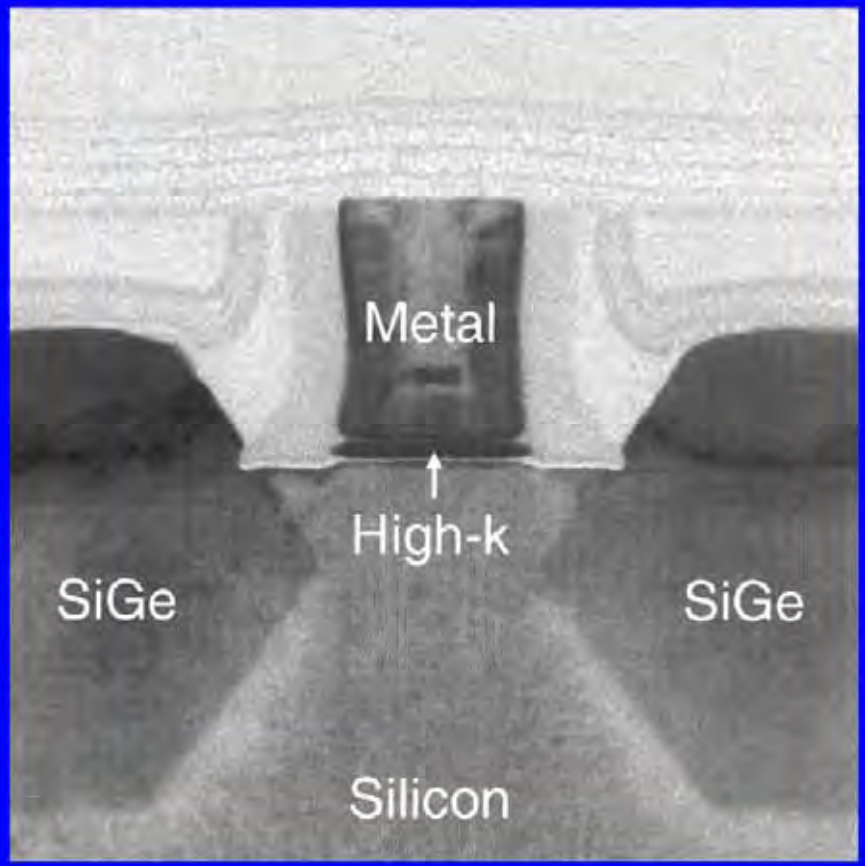
NMOS I_{DSAT} vs. I_{OFF}



1.36 mA/μm at I_{OFF} = 100 nA/μm

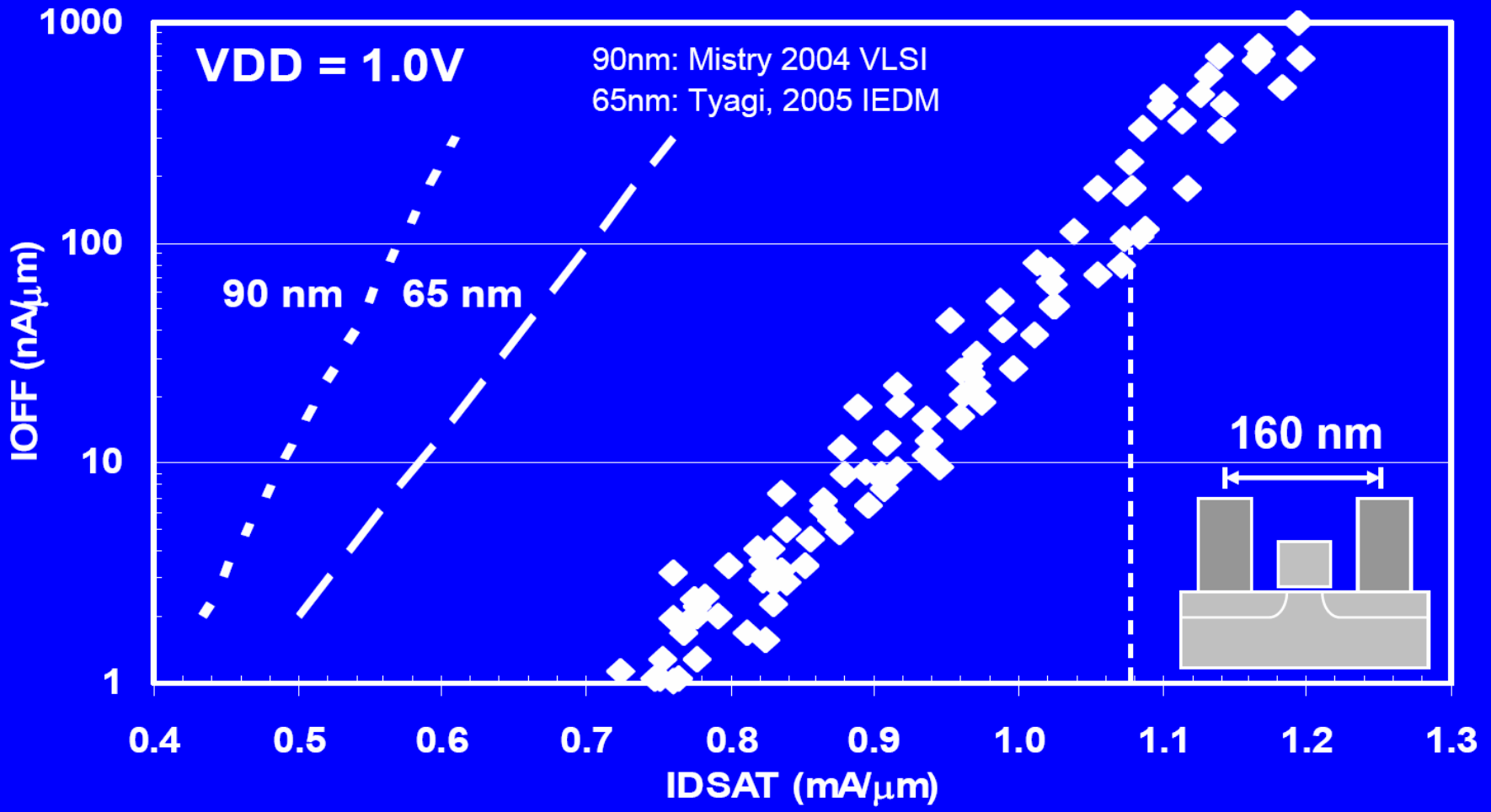
12% better than 65 nm

3RD Generation Strained Silicon



- Increased Ge fraction
  - 90 nm: 17% Ge
  - 65 nm: 23% Ge
  - 45 nm: 30% Ge
- SiGe closer to channel

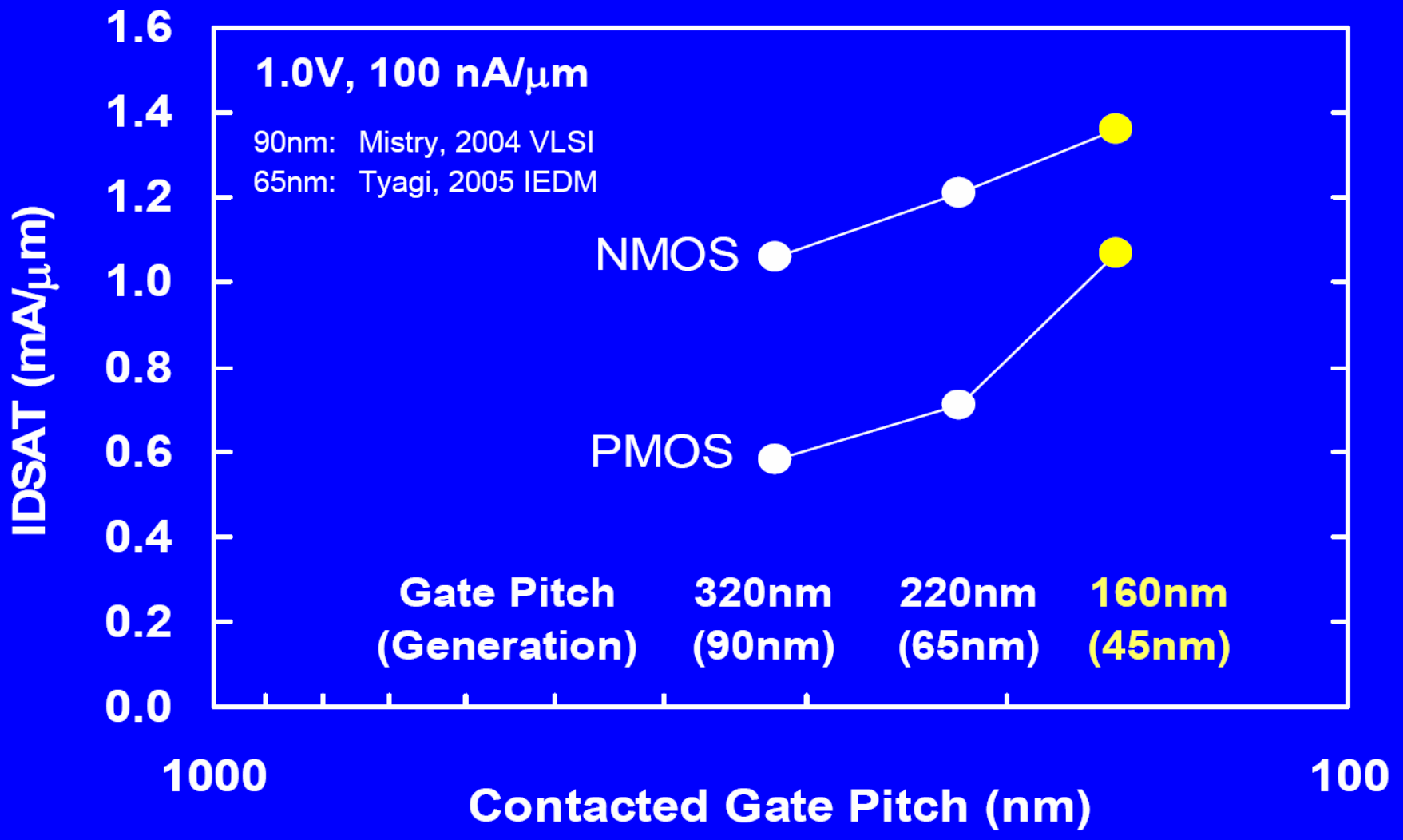
PMOS I_{DSAT} vs. I_{OFF}



1.07 mA/μm at I_{OFF} = 100 nA/μm

51% better than 65 nm

Transistor Performance vs. Gate Pitch

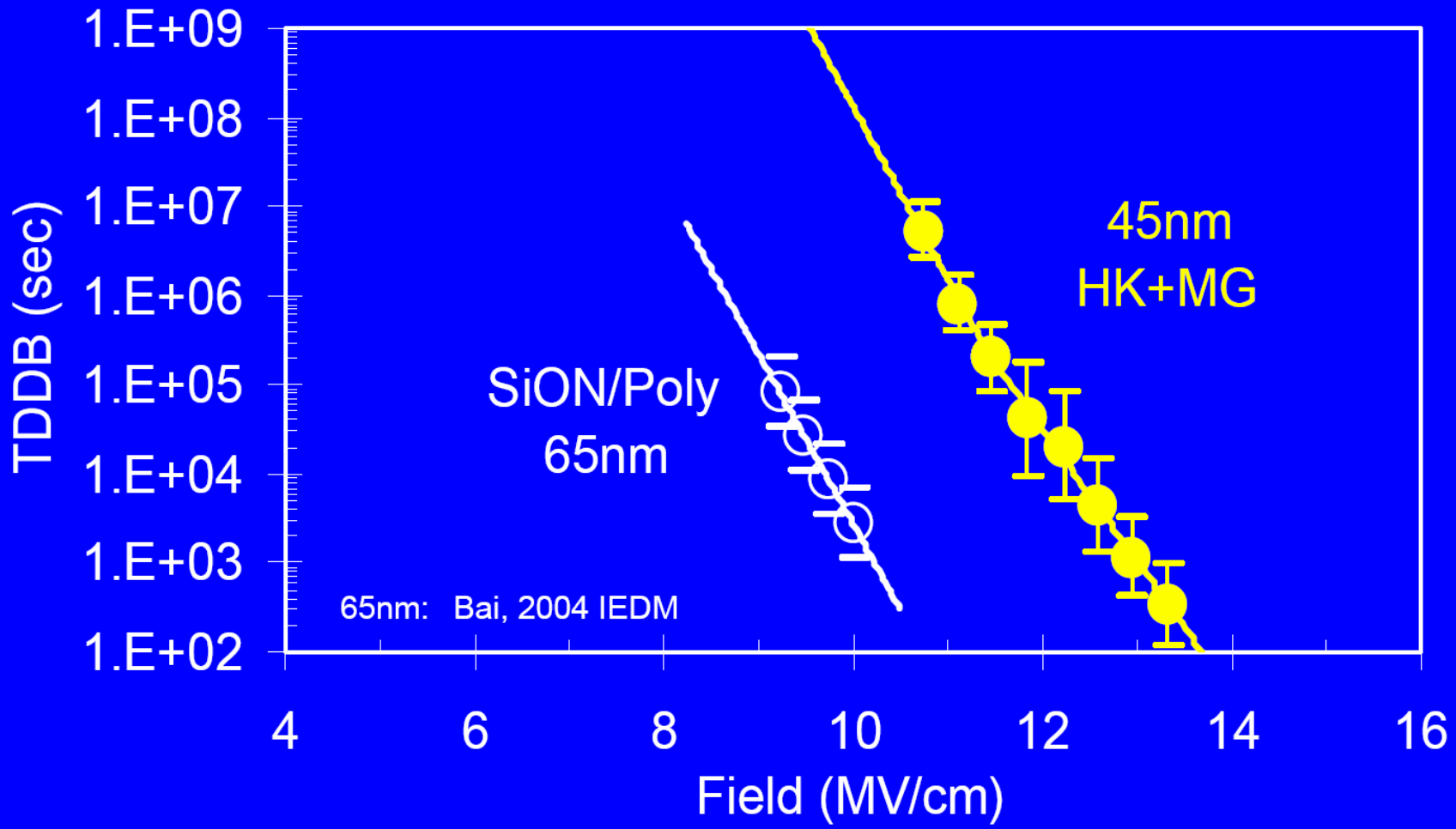


Simultaneous performance and density improvement

Transistor Reliability Challenges

- Defect types in SiO_2 have been studied for decades
- New defect types for high-k need to be suppressed
- T_{INV} scaled ~0.7X relative to 65 nm
  - Need to support 30% higher E-field

Transistor Reliability - TDDB*



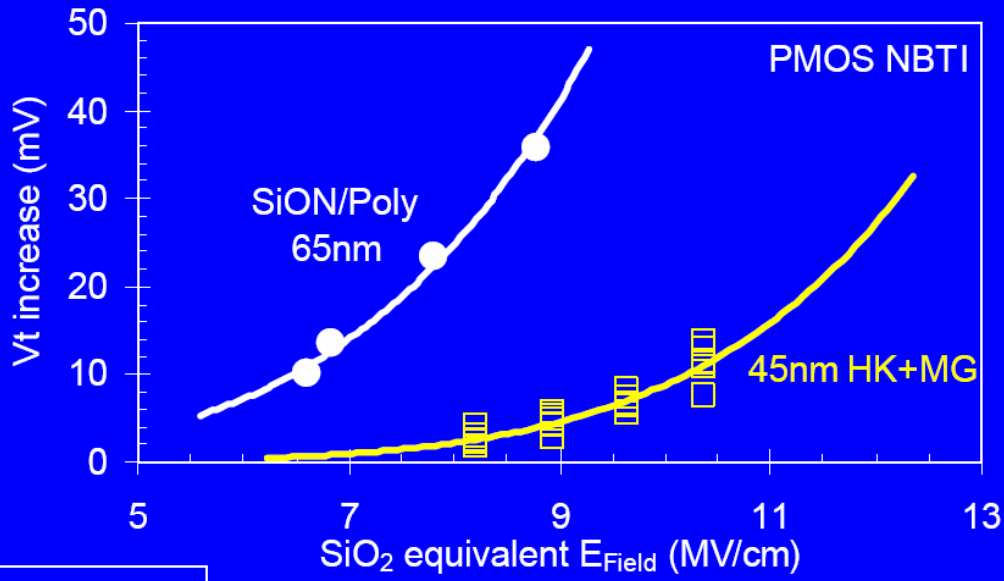
45nm High-k + Metal Gate supports 30% higher E-field

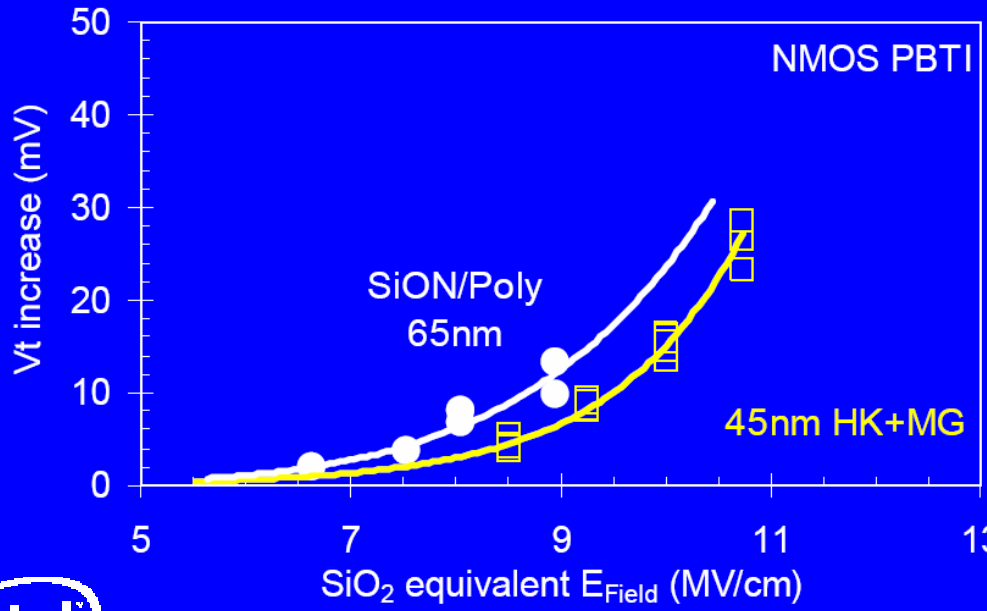
*Time Dependent Dielectric Breakdown

Transistor Reliability: Bias Temperature

PMOS NBTI

45 nm Hi-k + MG supports 50% higher E-field





NMOS PBTI

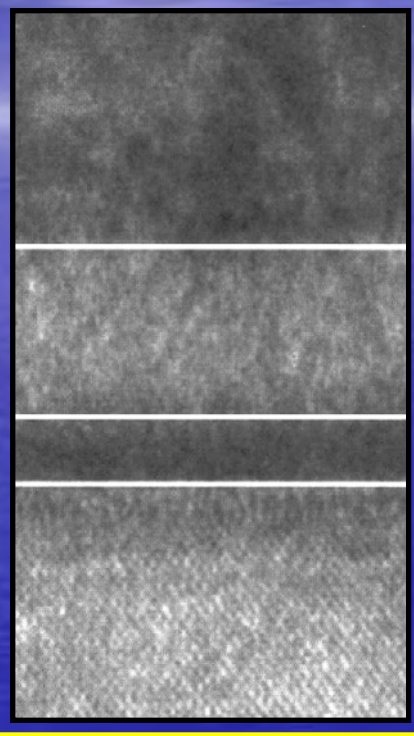
45 nm Hi-k + MG supports 15% higher E-field

65nm: Bai, 2004 IEDM

*N/P BTI=N/P Bias Temperature Instability IEDM 2007

High-k + Metal Gate Transistors

- ✓ Integrated 45 nm CMOS process
- ✓ High performance
- ✓ Low leakage
- ✓ Meets reliability requirements
- ✓ Manufacturable in high volume



Low Resistance Layer

Work Function Metal
Different for NMOS and PMOS

High-k Dielectric
Hafnium based

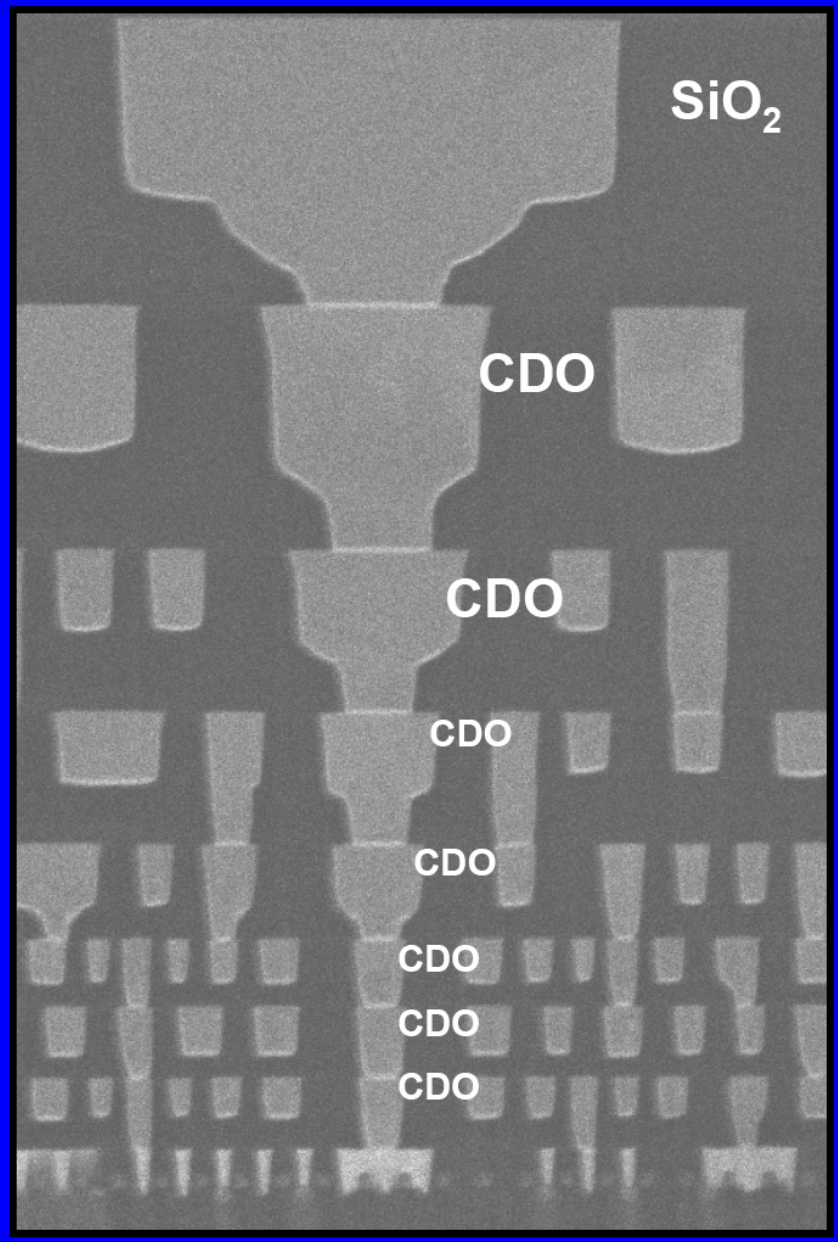
Silicon Substrate

"The implementation of high-k and metal gate materials marks the biggest change in transistor technology since the introduction of polysilicon gate MOS transistors in the late 1960s"

Gordon Moore

Interconnects

- Metal 1-3 pitches match transistor pitch
- Graduated upper level pitches optimize density & performance
- Lower layer SiCN etch stop layer thinned 50% relative to 65 nm
- Extensive use of low-k ILD



Beyond 45nm …

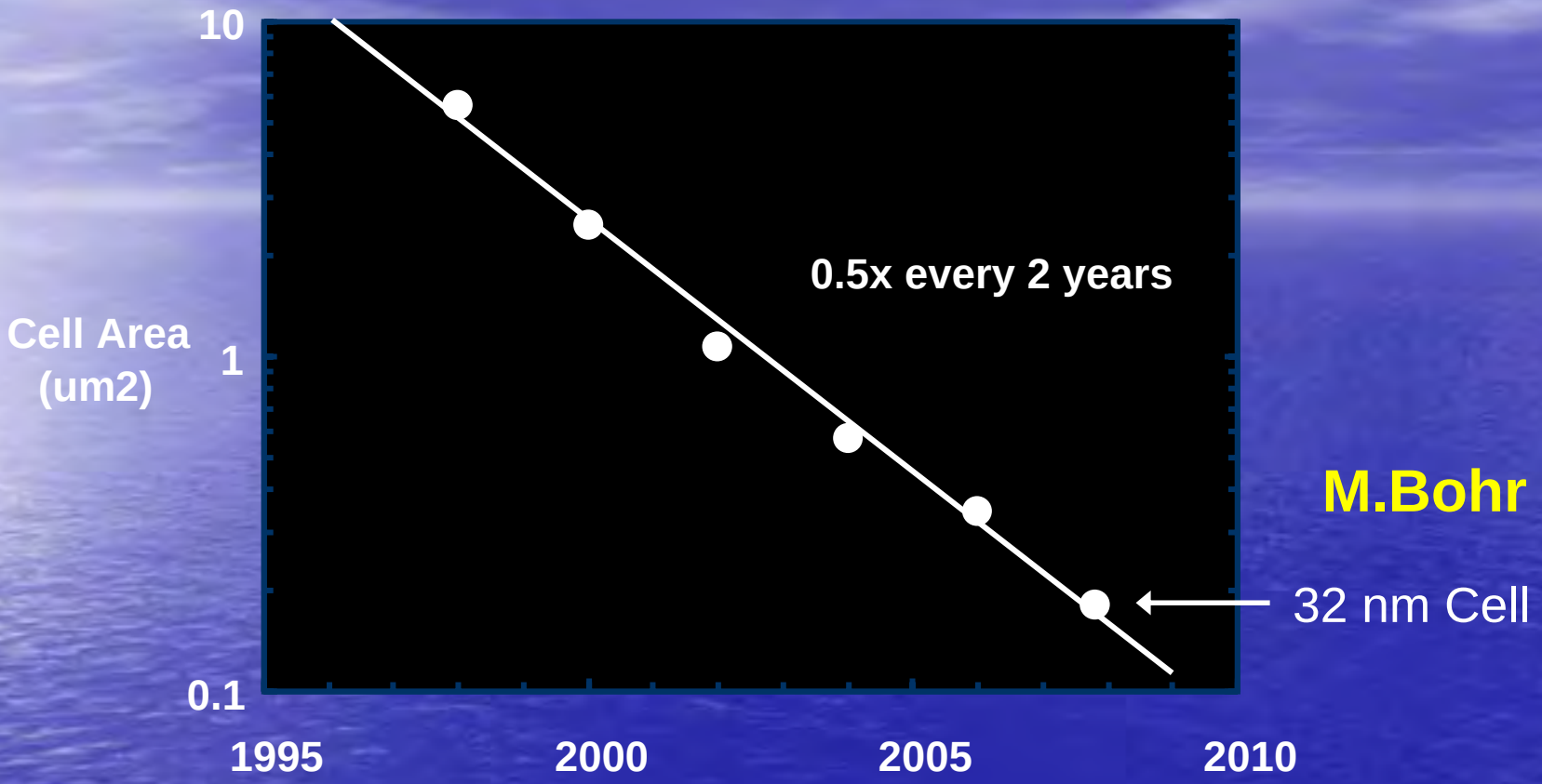
Intel First to Demonstrate Working 32 nm SRAM + Logic Chips

M.Bohr

September 18th, 2007

2008 ISS US

Intel SRAM Cell Size Trend



The smaller the SRAM cell, the more transistors that can be packed on a chip and utilized for more features

Transistor density continues to double every 2 years

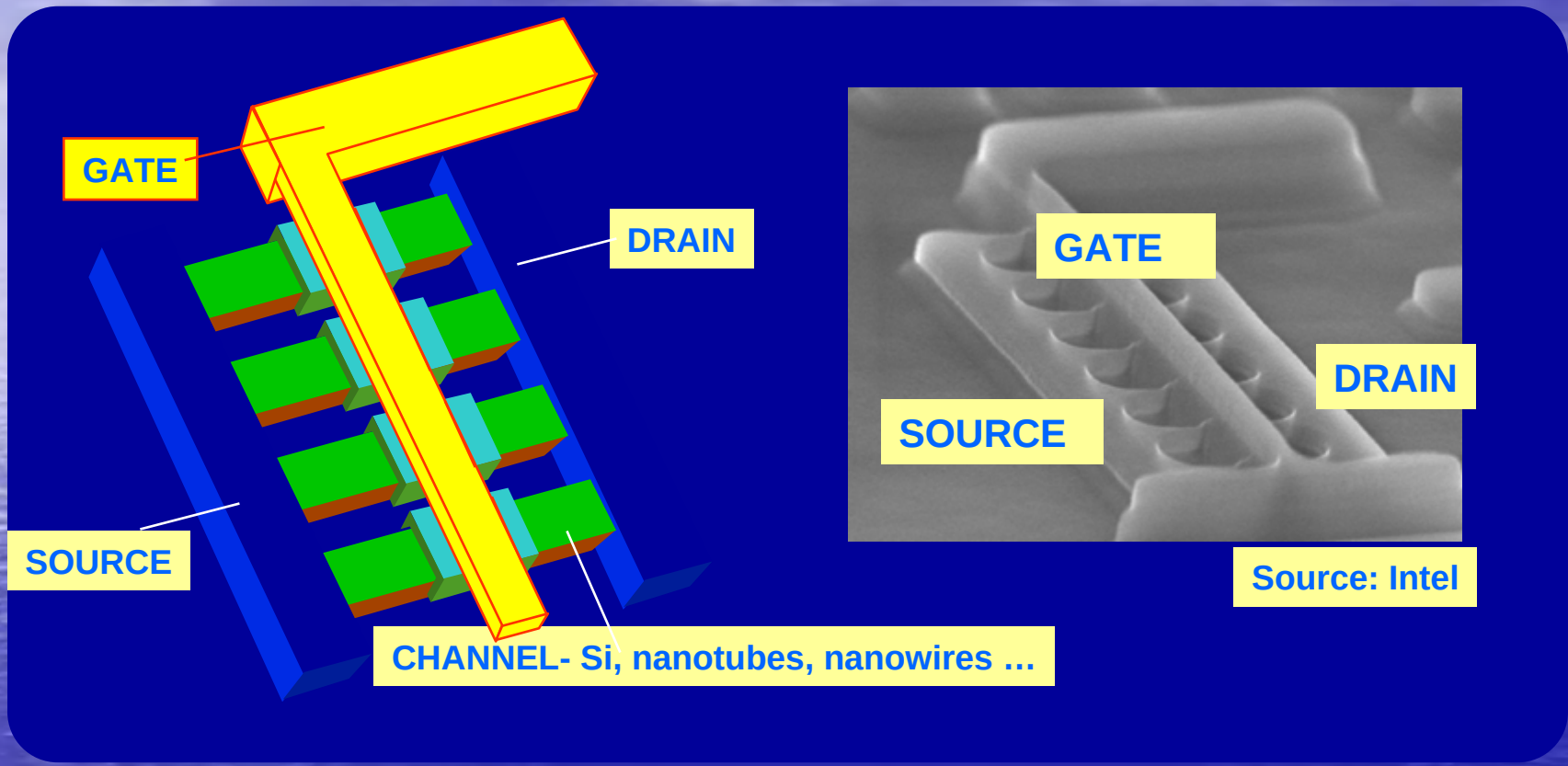
September 18th, 2007

2008 ISS US

Agenda

- Yesterday
- Today
- Tomorrow
- The Day after Tomorrow

Tri-Gate Transistor:
"A template for the future"



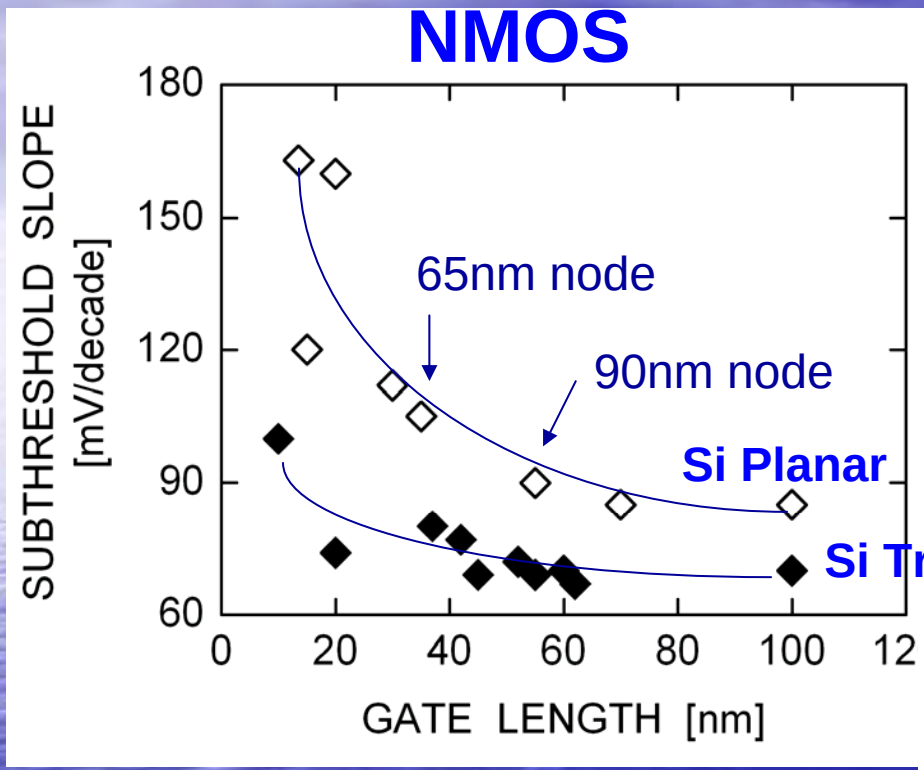
Technical details presented at:

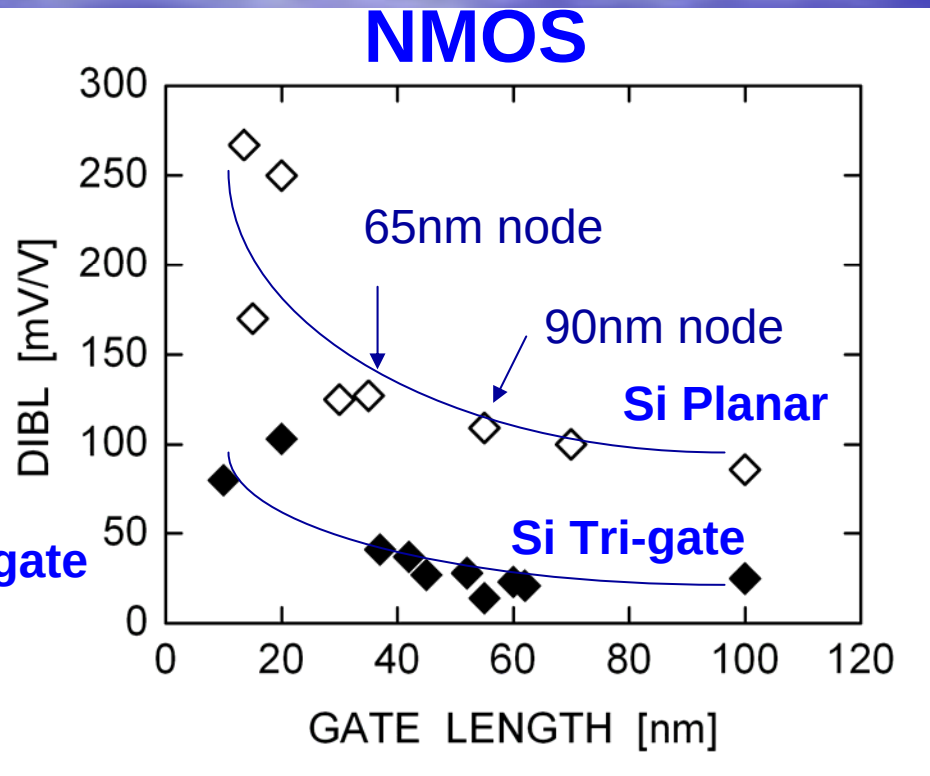
ISSDM Conference, Japan, Sept 17, 2002

R.Chau

2008 ISS US

Benefits of Tri-Gate architecture

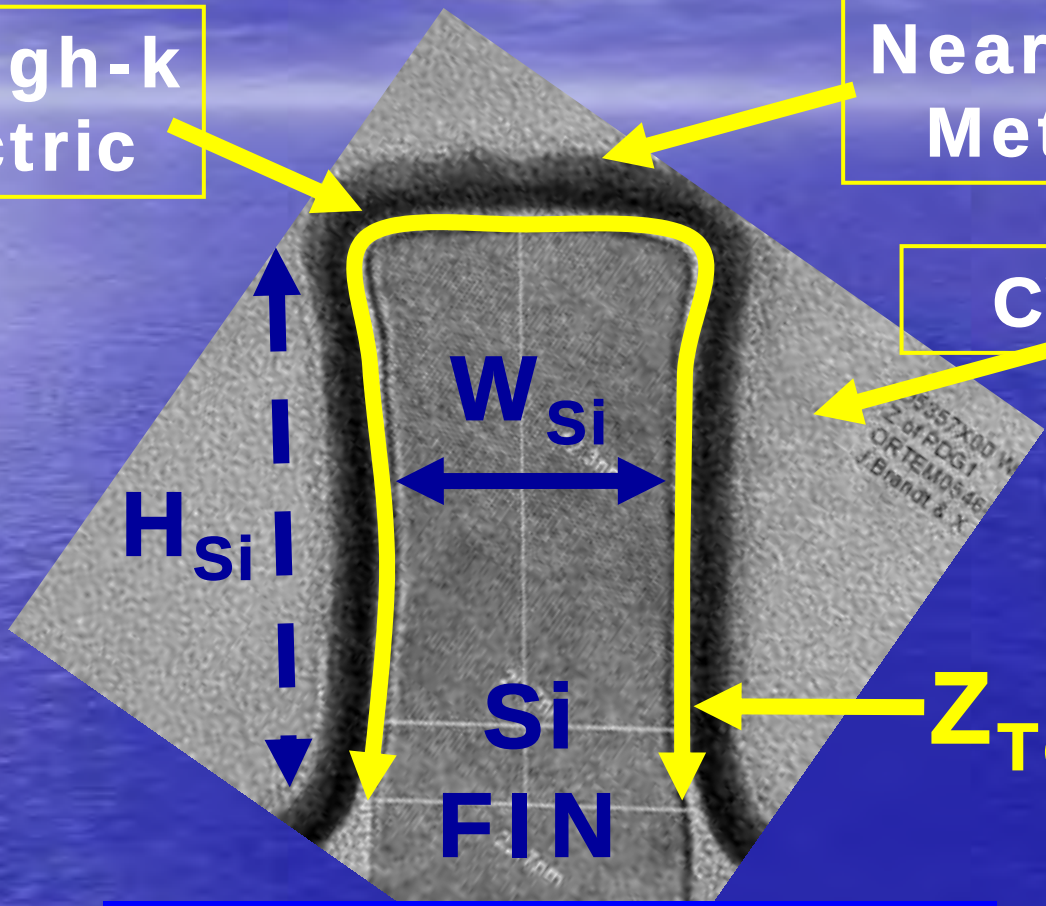




- Si planar transistors become exceedingly hard to scale
- Tri-gate architecture improves electrostatics significantly and extends transistor scalability

2008 ISS US R.Chau

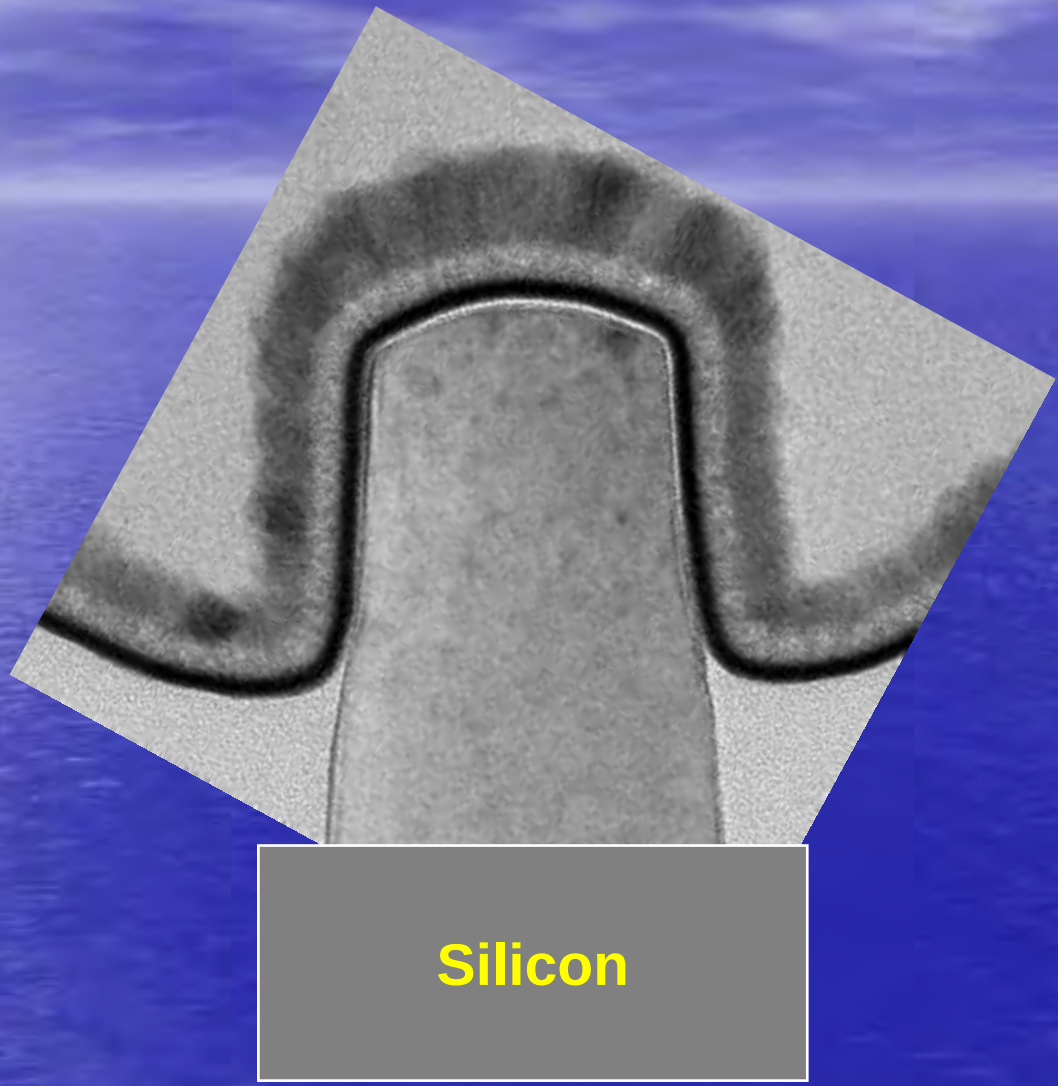
Tri-Gate FIN Critical Dimensions



VLSI Symposium, 6-2006

2006 T33 03

Tri-Gate On Bulk!



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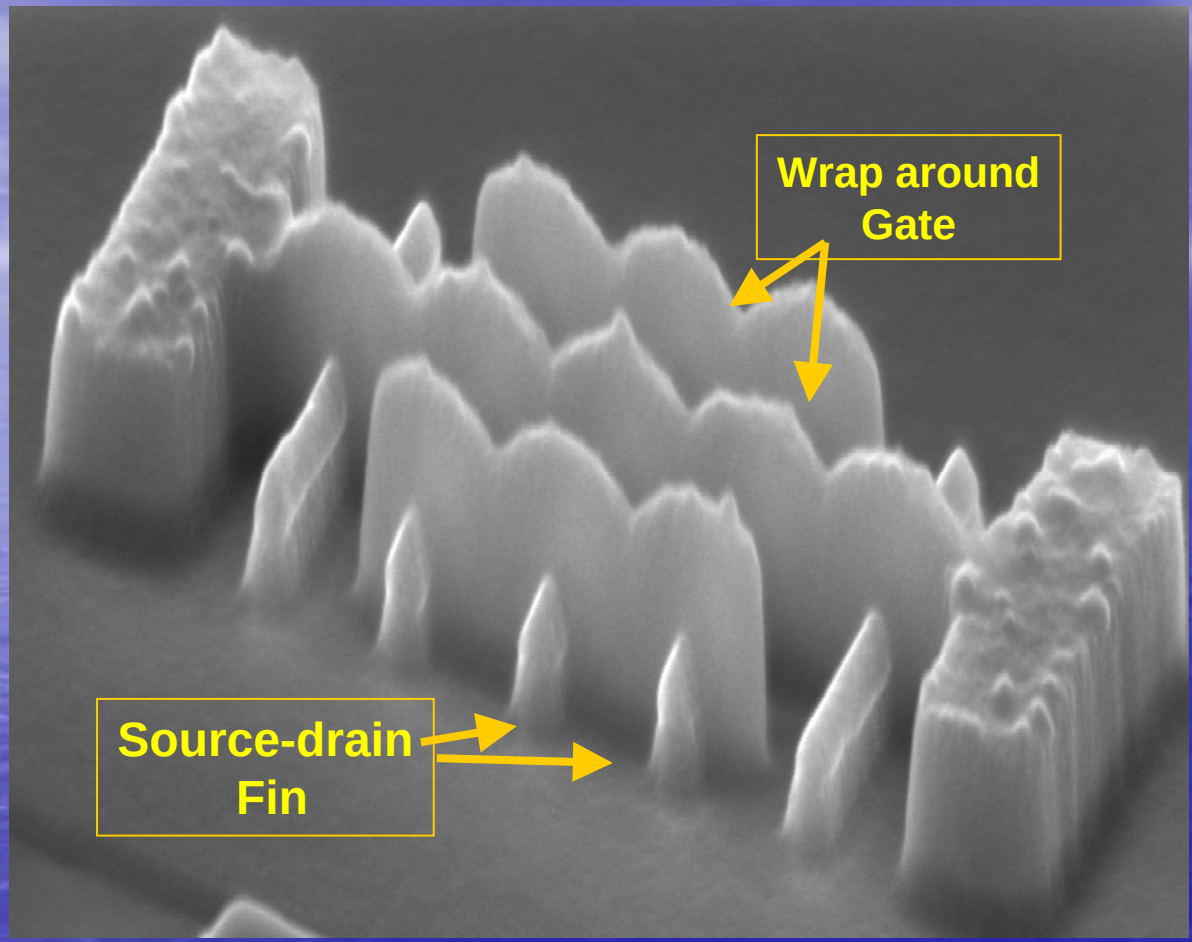
VLSI Symposium, 6-2006

The Key is Optimizing the Integration



1. Tri-gate gives better off current and therefore less wasted power
2. High k – metal gate gives both higher speed and less wasted power
3. Strained Si produces higher speed and less wasted power

The sum of all these pieces is once again world leading transistors

Agenda

- Yesterday
- Today
- Tomorrow
- The Day after Tomorrow

The Hunt for Mobility

$$I_{DSAT} \propto \frac{W}{L} \cdot \mu \cdot C_{OX}$$

Picking the Right High-μ Material

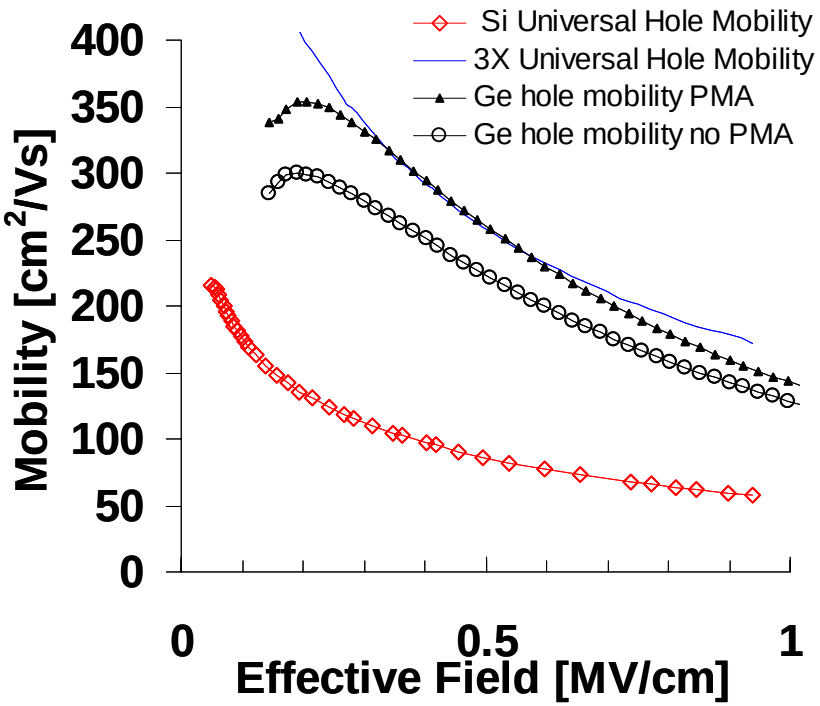
Material ⇒ Property ⇓	Si	Ge
Electron mobility	1600	3900
Hole mobility	430	1900
Bandgap (eV)	1.12	0.66
Dielectric constant	11.8	16

Why Ge?

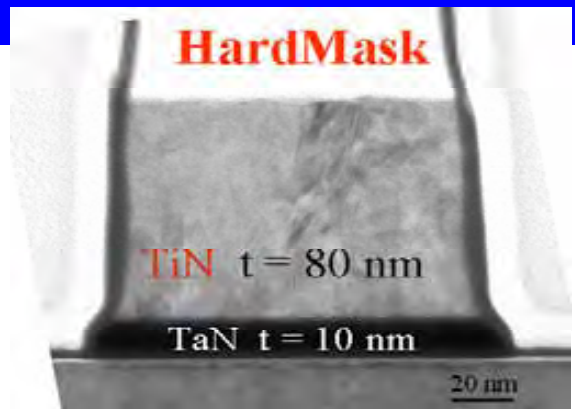
- **More symmetric and higher carrier mobilities**
  - **Highest hole mobility**
- **Easier integration on Si**
- **Lower temperature processing**

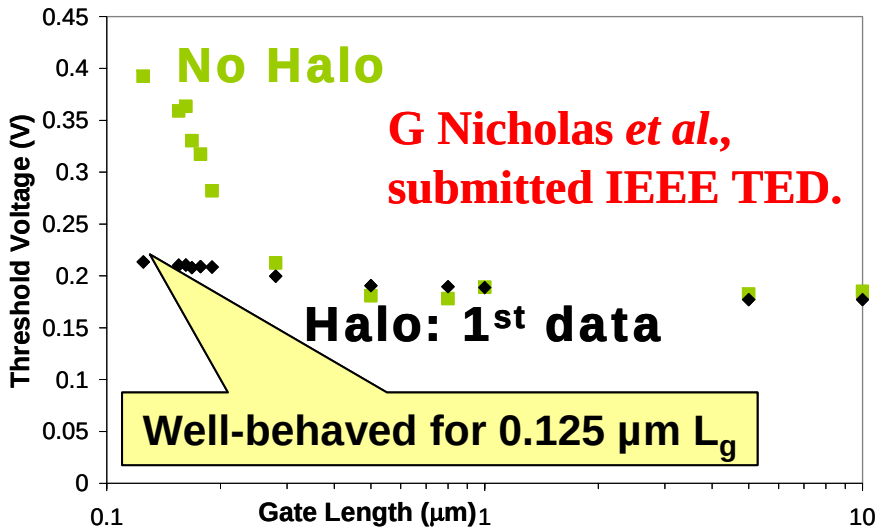
IMEC Ge pMOSFET

IMEC: M Meuris, M Heyns Intel: D Brunco, P Zimmerman



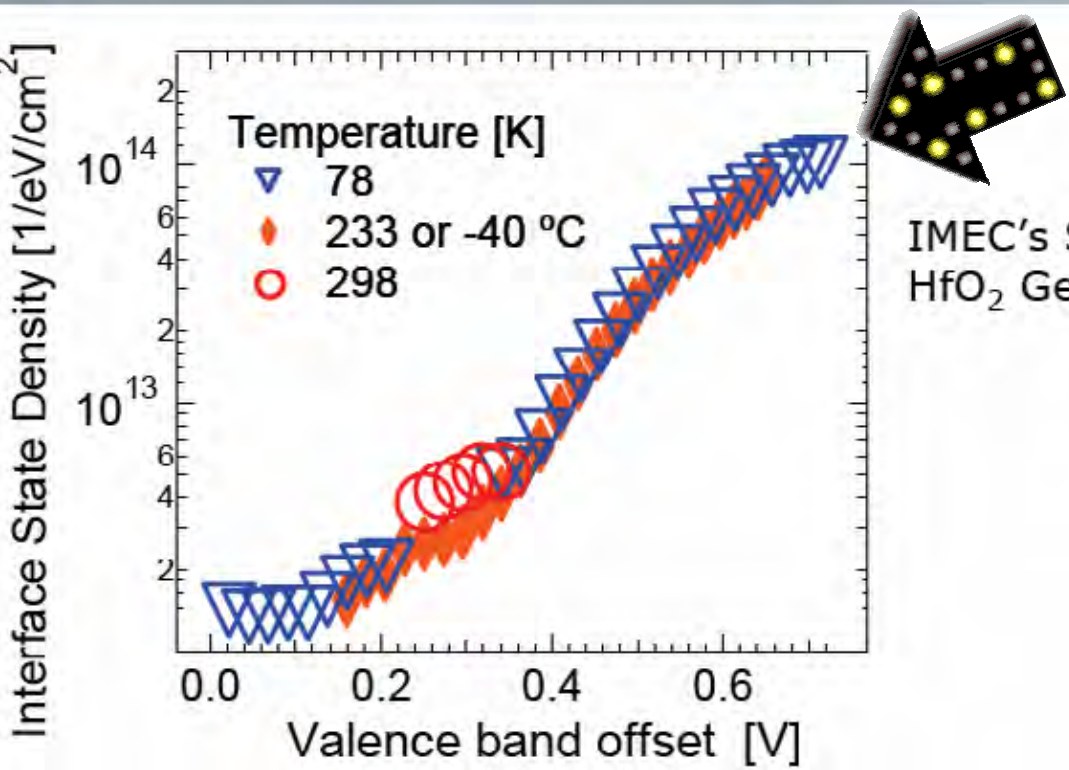
P Zimmerman *et al.*, IEDM 2006





- Ge pMOS mobilities up to 358 cm²/Vs at 12 Å EOT with a gate leakage less than 0.01 A/cm² at V_t + 0.6 V. (6 ML of Epi-Si)
- High performance Ge pMOS transistors with L_g from 10 to 0.125 µm. (future target L_g to 50 nm)

Full conductance measurement at low temperature allows correct interface trap density extraction



IMEC's Si-passivated HfO_2 Ge MOSFETs

Acceptor type interface traps near the conduction band explain

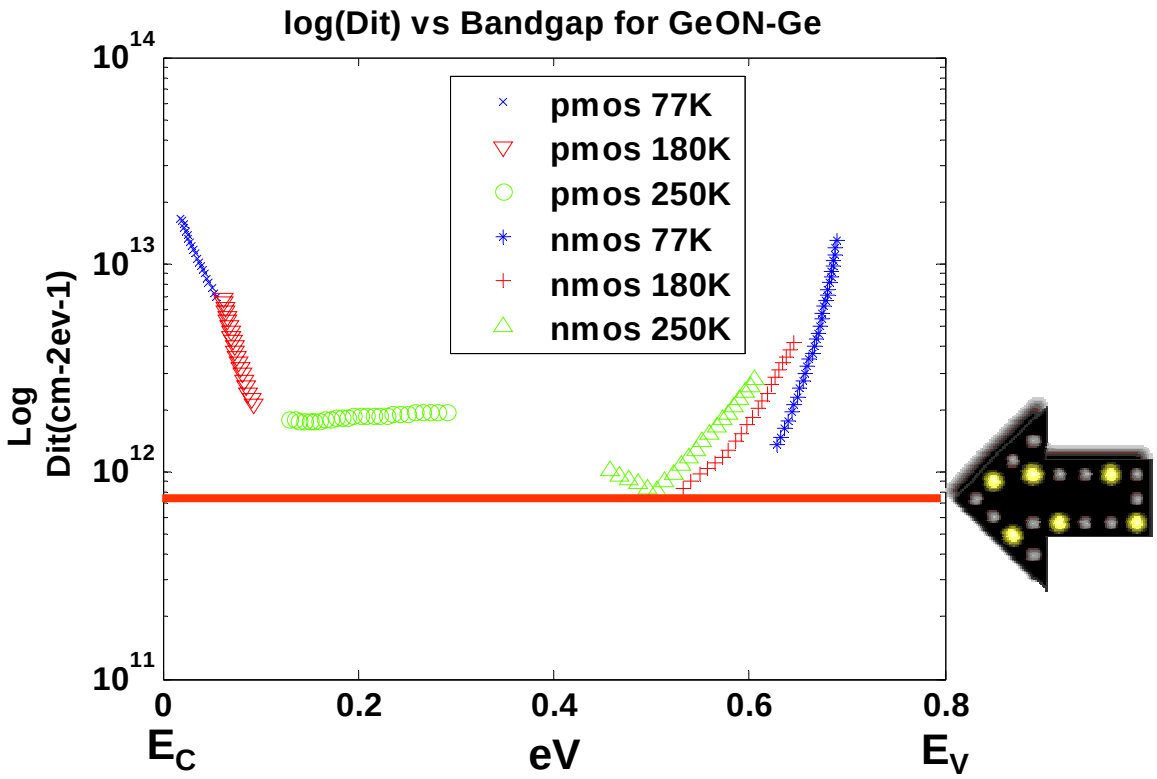
good performing pMOS

traps are neutral and don't severely reduce channel mobility

and bad performing nMOS

charged traps reduce mobility and lower amount of free carriers

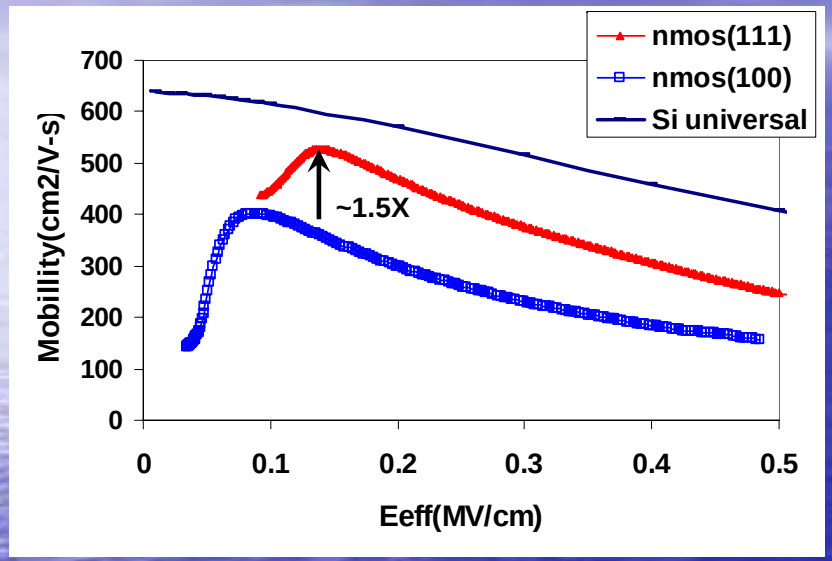
Reducing Ge surface states



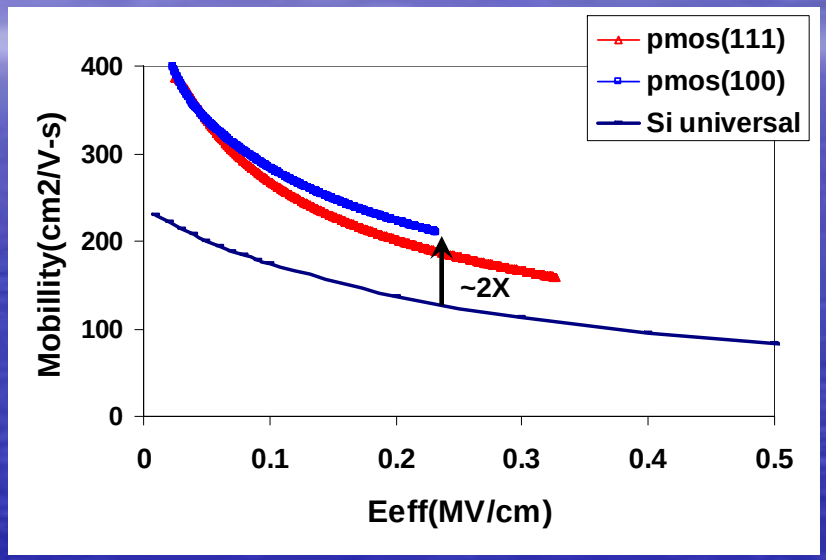
D. Kuzum, et al., *IEEE IEDM* Dec. 2007

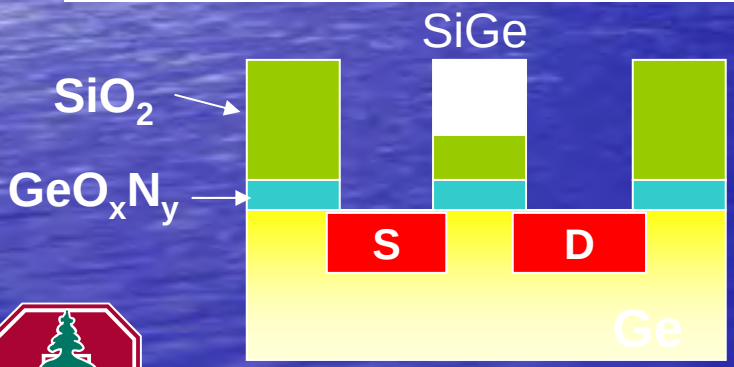
Ge N- and P-MOS Mobility with GeO_xN_y

Electron Mobility



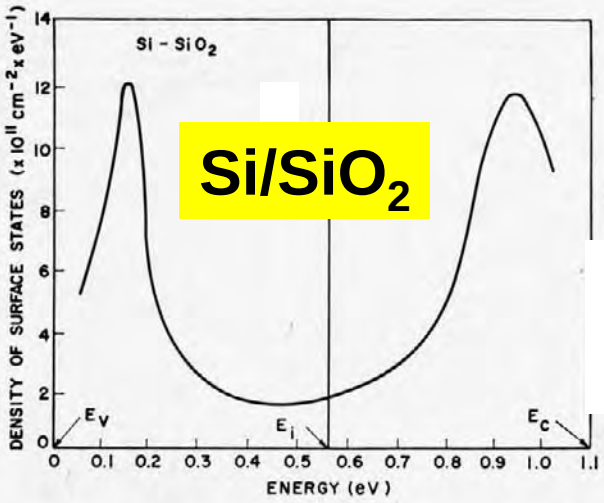
Hole Mobility





- Highest μ_n reported so far
- (111) gives ~50%high μ_n
- Need further improved dielectric stack to achieve high μ_n

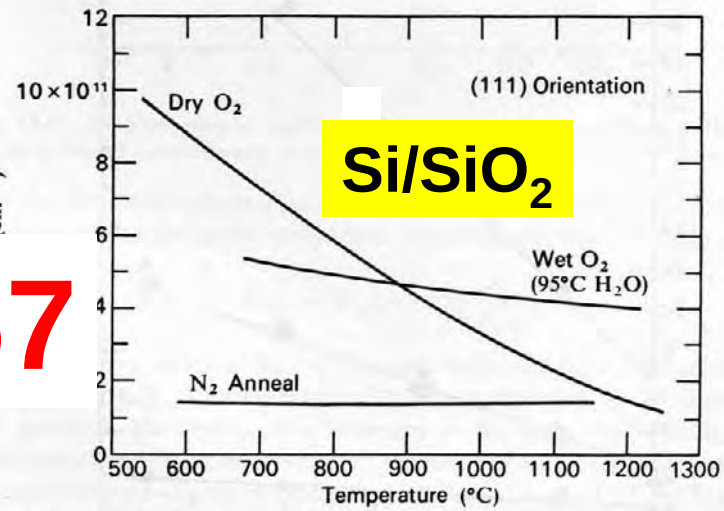
D. Kuzum, et al., *IEEE IEDM* Dec. 2007



Si/SiO$_2$

Fig. 21 Surface-state density of a Si-SiO$_2$. Near the band edges the temperature method is used. At the midgap the conductance method is used. (Ref. 9.)

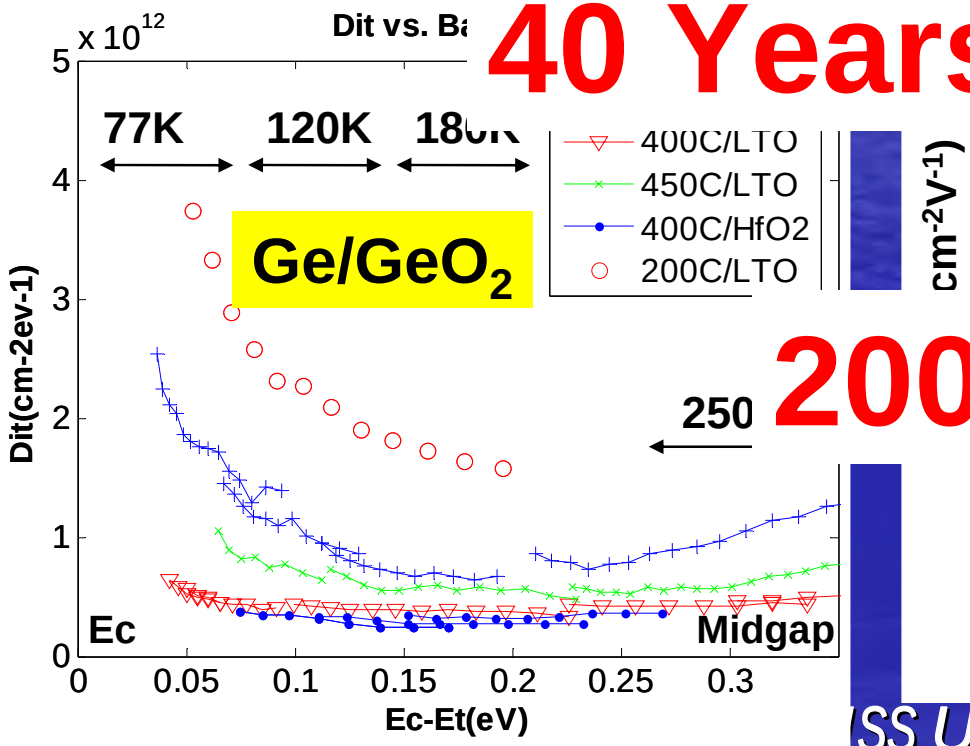
1967



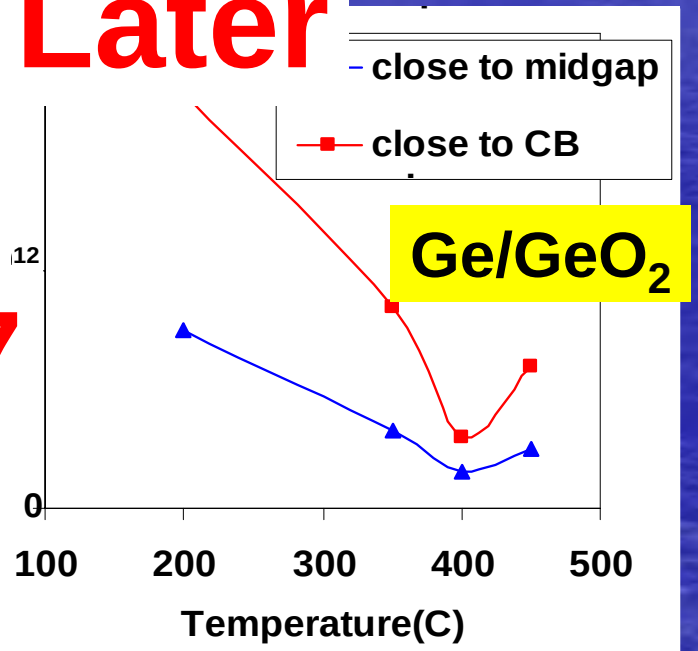
Si/SiO$_2$

Fig. 12.8 Dependence of the surface-state charge density on the ambient and temperature of the final heat treatment.[15]

40 Years Later



2007



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Increasing Electron Mobility

Increased mobility in the transistor channel leads to higher performance and less energy consumption

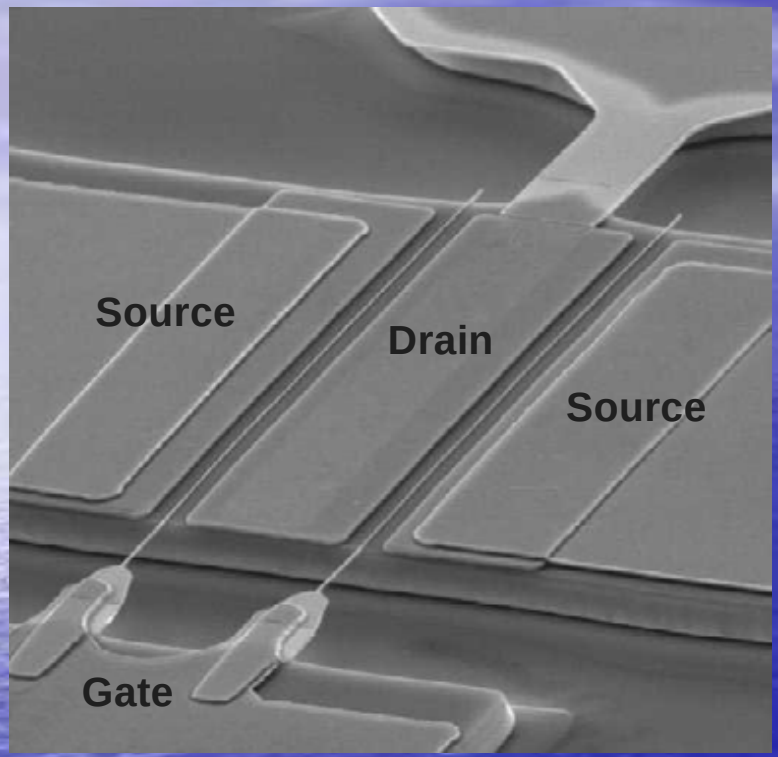
$$I_{DSAT} \propto \frac{W}{L} \cdot \mu \cdot C_{OX}$$

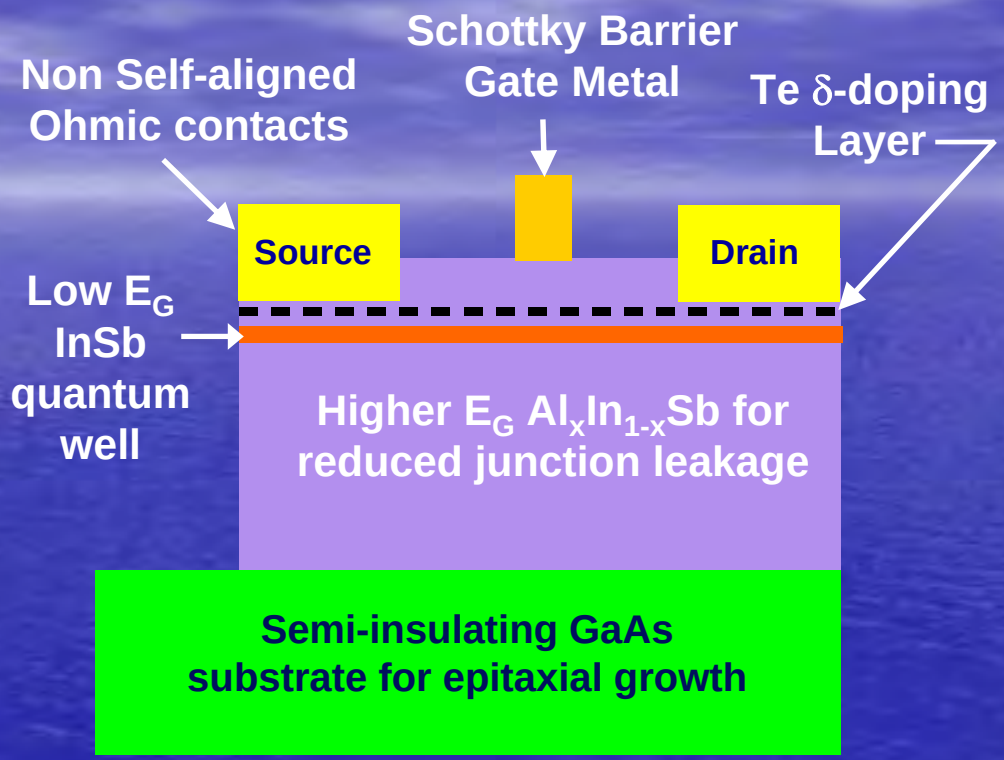
Relative mobility

	Compound Semiconductors		
Si	**GaAs**	**InAs**	**InSb**
1	**8**	**33**	**50**

Compound semiconductors have higher electron mobility than Si; InSb (indium antimonide) is highest of all

InSb QW* Transistor Fabrication





A two gate finger InSb QW transistor (QWFET*) is fabricated with gate air-bridge using mesa isolation

*QW = Quantum Well

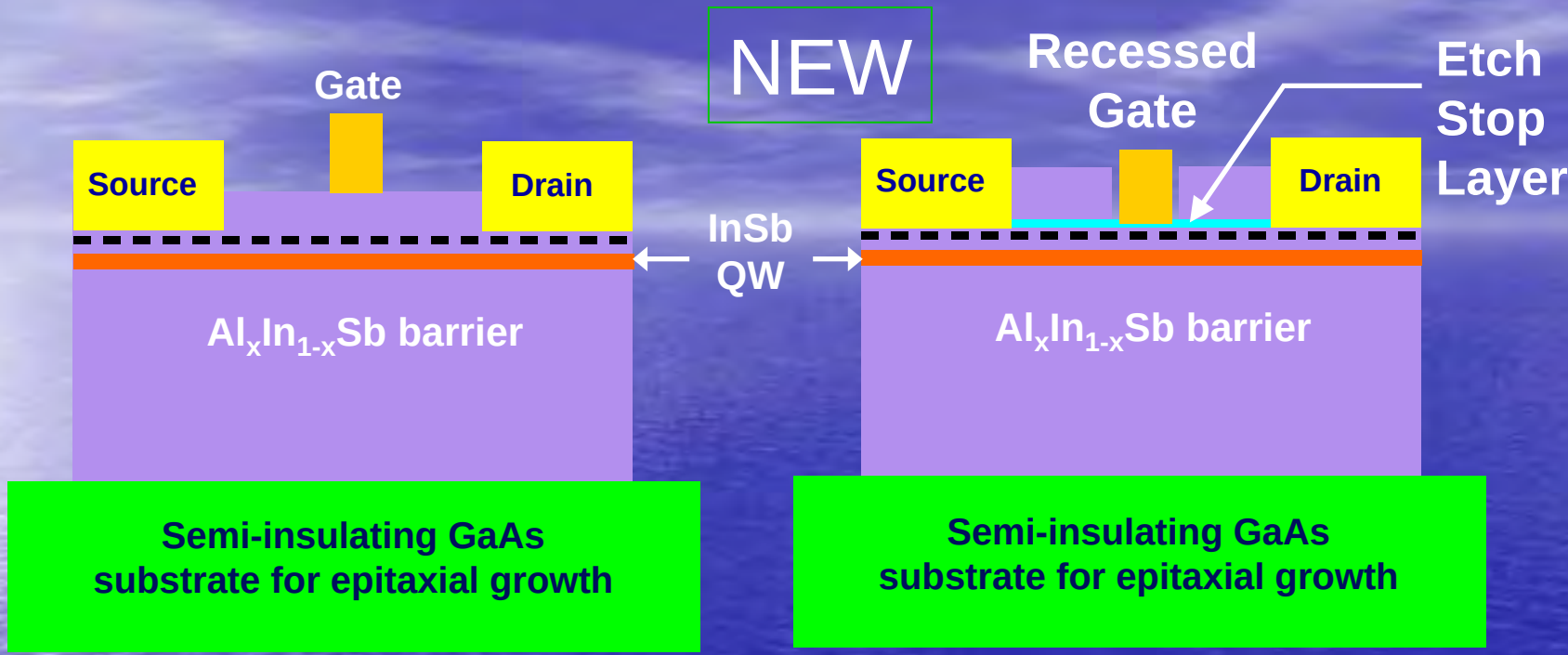
*FET = Field-effect Transistor

Source: Intel

IEDM 2004

2008 ISS US

Depletion and Enhancement Mode



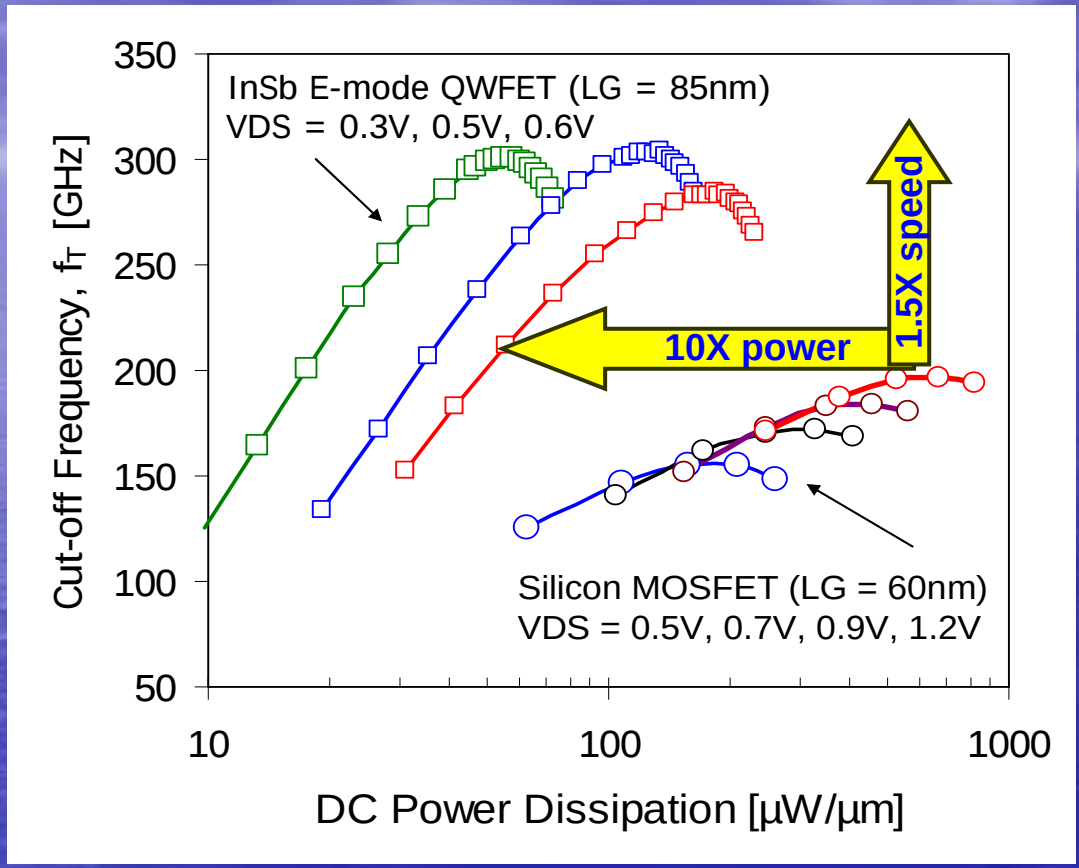
Depletion mode (Normally ON)

Enhancement mode (Normally OFF)

A novel gate recess process is used to fabricate enhancement mode InSb QWFETs

IEDM 2005

Speed, Power, Performance



InSb QWFETs show > 10x reduction in active power dissipation compared to Si MOSFETs

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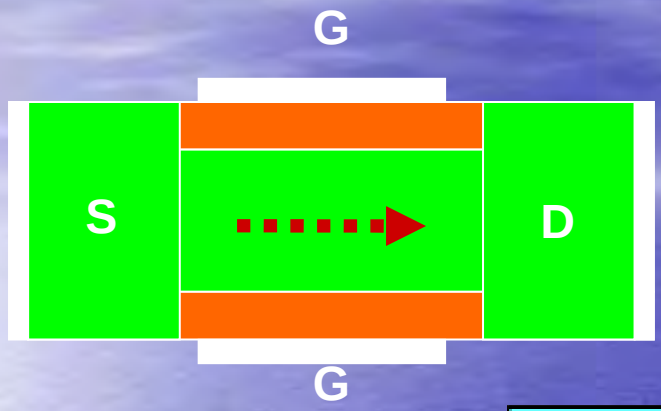
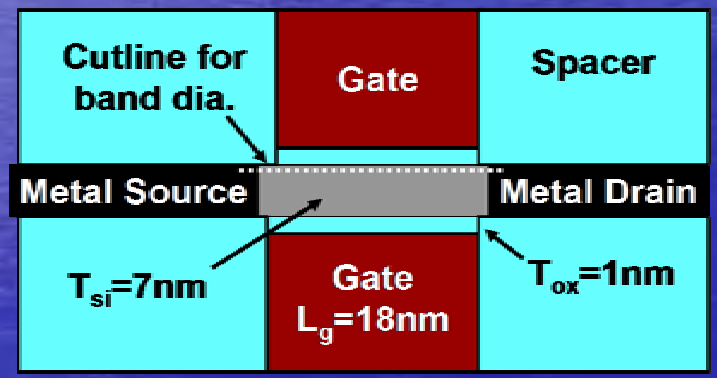
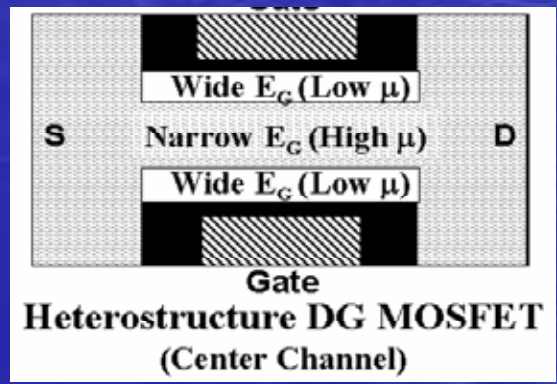
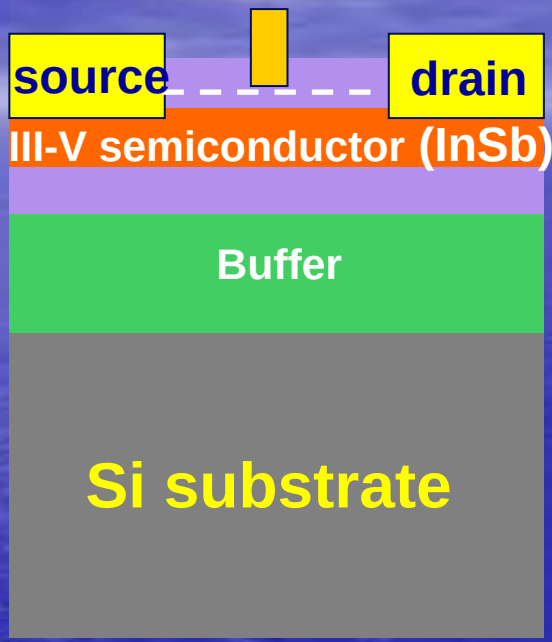
Engineering Trade offs







Integration on Si Platform



Current research on incorporation of new transistor onto the existing Si platform

March 2006

2008 ISS US

Heterogeneous Integration of Enhancement Mode $In_{0.7}Ga_{0.3}As$ Quantum Well Transistor on Silicon Substrate using Thin (≤ 2 μm) Composite Buffer Architecture for High-Speed and Low-voltage (0.5V) Logic Applications

M. K. Hudait, G. Dewey, S. Datta, J. M. Fastenau*, J. Kavalieros, W. K. Liu*, D. Lubyshev*, R. Pillarisetty, W. Rachmady, M. Radosavljevic, T. Rakshit and Robert Chau
Technology and Manufacturing Group, Intel Corporation, Hillsboro, OR-97124, USA
*IQE Inc, Bethlehem, USA
Contact: robert.s.chau@intel.com

Abstract

This paper describes for the first time, the heterogeneous integration of $In_{0.7}Ga_{0.3}As$ quantum well device structure on Si substrate through a novel, thin composite metamorphic buffer architecture with the total composite buffer thickness successfully scaled down to 1.3μm, resulting in high-performance short-channel enhancement-mode $In_{0.7}Ga_{0.3}As$ QWFETs on Si substrate for future high-speed digital logic applications at low supply voltage such as 0.5V.

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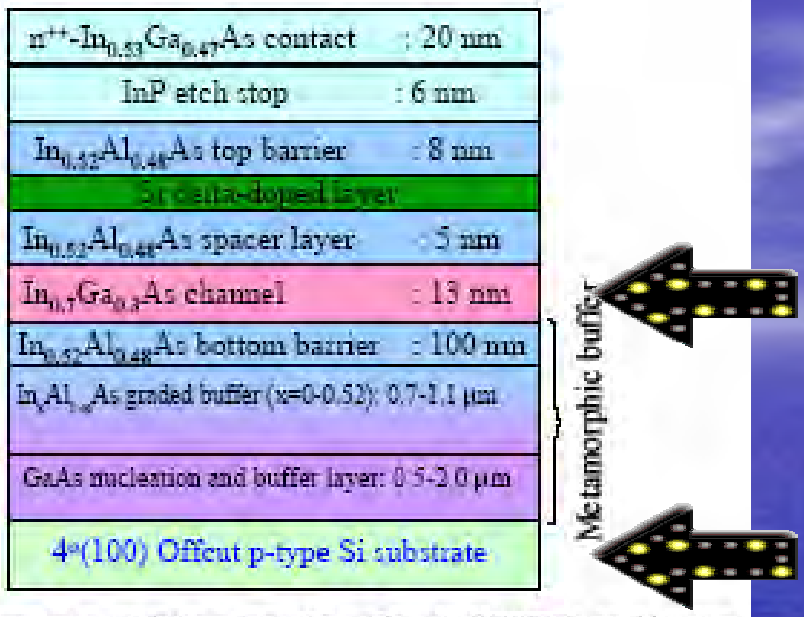

Fig.1: Heterogeneous integration of $In_{0.7}Ga_{0.3}As$ QWFETs on Si using metamorphic composite buffer architecture consisting of GaAs and $In_xAl_{1-x}As$ graded buffer layers. The composite buffer in this work has total thickness in the range of 1.3μm to 3.2μm.

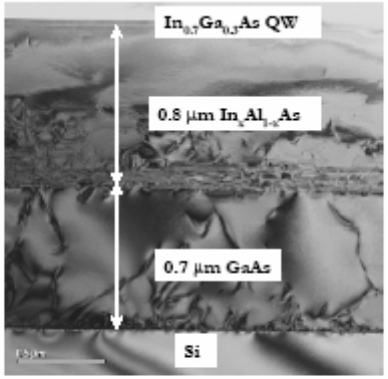

Fig. 2a: Cross-sectional TEM image of $In_{0.7}Ga_{0.3}As$ QWFET on Si using 1.5μm composite buffer. The misfit and threading dislocations are predominantly contained in the composite buffer, with the $In_{0.7}Ga_{0.3}As$ QW virtually defect-free.

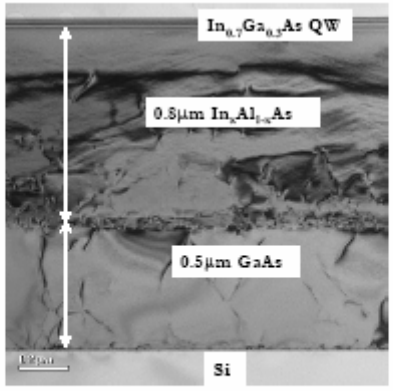

Fig. 2b: Cross-sectional TEM image of $In_{0.7}Ga_{0.3}As$ QWFET on Si using composite buffer with total thickness of 1.3μm. The active $In_{0.7}Ga_{0.3}As$ QW is virtually defect-free.

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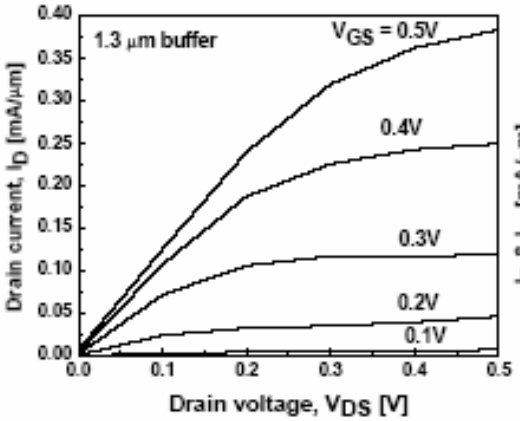

Fig.8: I_D-V_{DS} characteristics of enhancement-mode L_G=80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with 1.3μm composite buffer at room temperature.

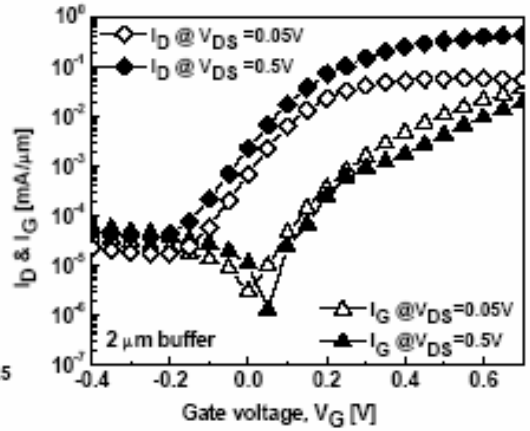

Fig. 9a: Drain current (I_D) and gate leakage (I_G) versus V_G of enhancement-mode L_G=80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with 2μm composite buffer at room temperature. V_T = + 0.07V, I_{Dsat} = 0.25mA/μm, I_{ON}/I_{OFF} = 2500 at V_{DS}=0.5V with 0.5V V_G swing.

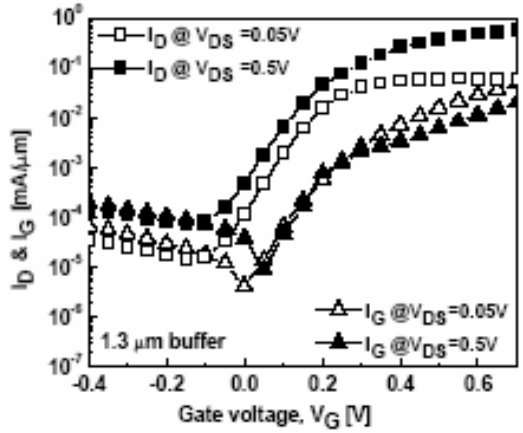

Fig. 9b: Drain current (I_D) and gate leakage (I_G) versus V_G of enhancement-mode L_G=80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with 1.3μm composite buffer at room temperature. V_T = +0.11V, I_{Dsat} = 0.32mA/μm, I_{ON}/I_{OFF} = 2150 at V_{DS}=0.5V with 0.5V V_G swing.

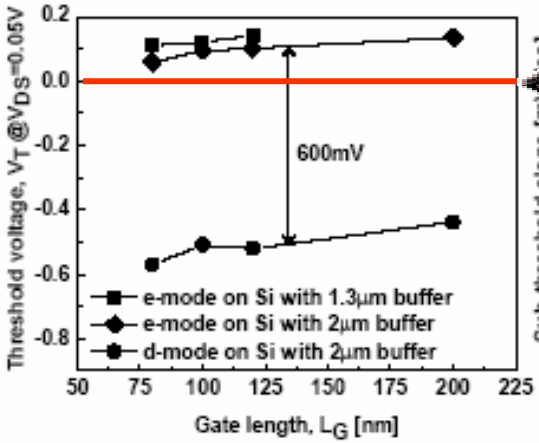

Fig. 10: Threshold voltage (V_T) as a function of L_G for enhancement-mode (e-mode) and depletion-mode (d-mode) $In_{0.7}Ga_{0.3}As$ QWFETs on Si. Positive V_T shift of about 600mV from d-mode operation to e-mode operation was accomplished through gate recess etch.

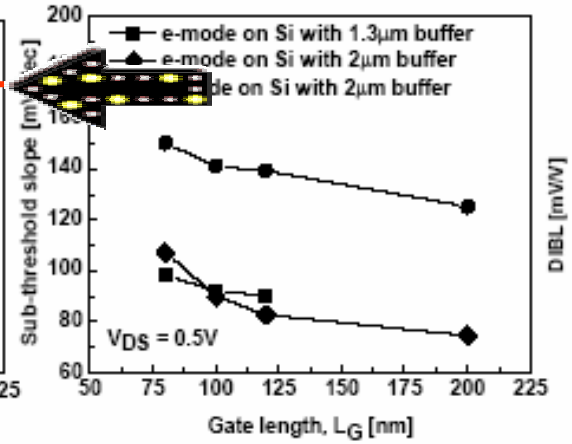

Fig. 11: Sub-threshold slope (SS) as a function of L_G for e-mode and d-mode $In_{0.7}Ga_{0.3}As$ QWFETs on Si, showing improved SS of e-mode over d-mode devices due to shorter gate to channel separation in e-mode.

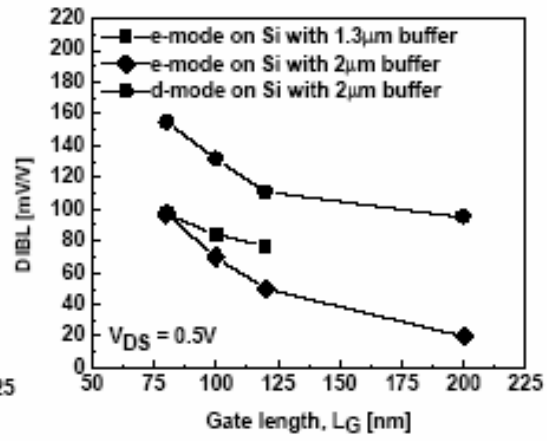

Fig.12: DIBL as a function of L_G for e-mode and d-mode $In_{0.7}Ga_{0.3}As$ QWFETs on Si, showing improved DIBL of e-mode devices over d-mode due to shorter gate to channel separation in e-mode.

The R&D Pipeline

Nat'l Labs
Supplier
Internal
Investme
Universit
Consortia

1-11nm

Extern Research

Materials
Equipment
Structures
Processes

16nm

22nm

32nm

45nm

Predevelopment

Development

Internal Research
RP1

Pathfinding
RP1/D1D

Development
D1D

Manufacturing
D1D/Fabs

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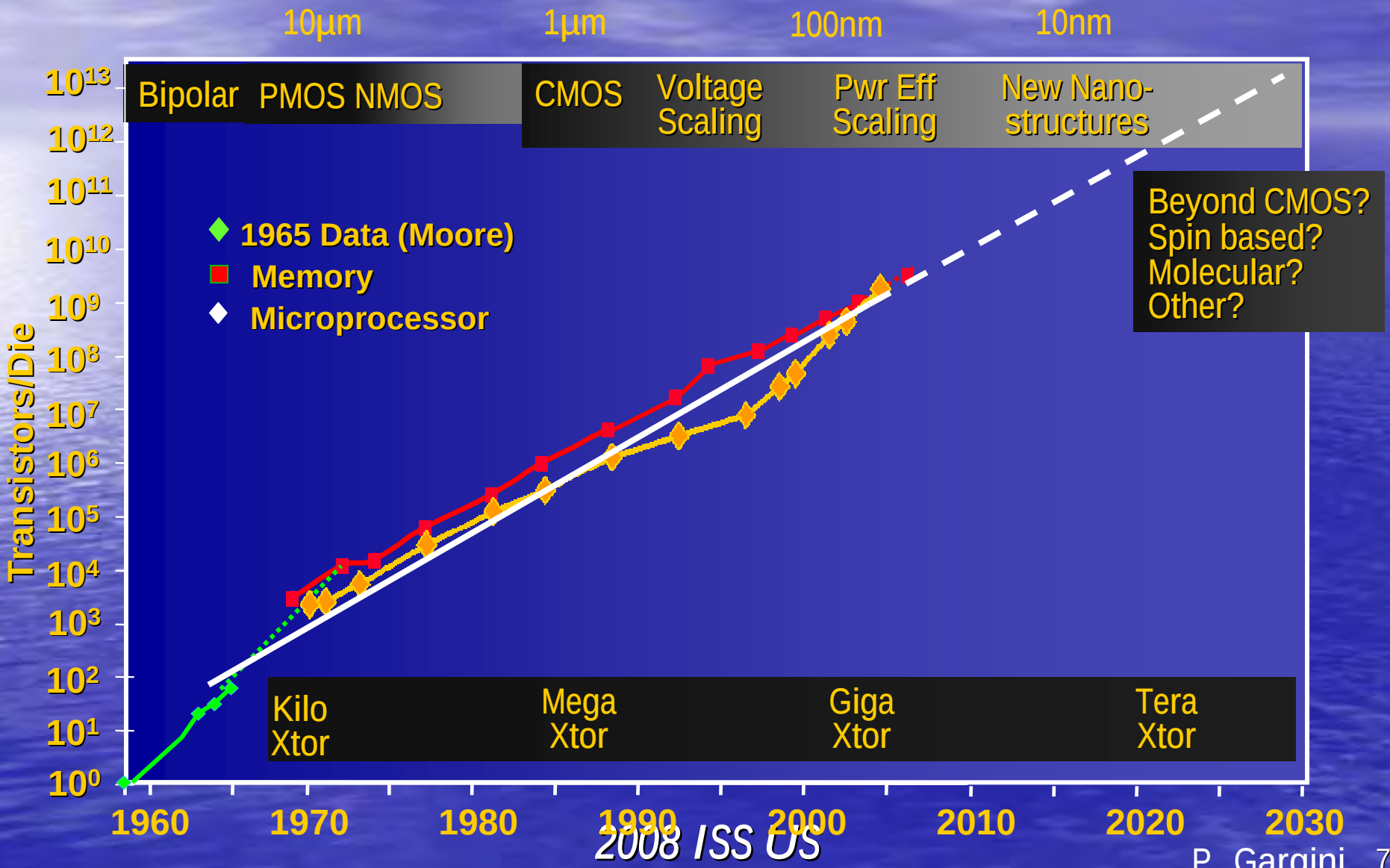

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Conclusions

- Multiple Technical Red Brick Walls of the past have been overcome
- Multiple viable technical options exist for the next 10-15 years
- Device technology will not be a show stopper for the foreseeable future